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Low trap states in *in situ* SiN_x/AlN/GaN metal-insulator-semiconductor structures grown by metal-organic chemical vapor deposition

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We report the use of SiN_x grown *in situ* by metal-organic chemical vapor deposition as the gate dielectric for AlN/GaN metal-insulator-semiconductor (MIS) structures. Two kinds of trap states with different time constants were identified and characterized. In particular, the SiN_x/AlN interface exhibits remarkably low trap state densities in the range of 10^{11}–$10^{12}\,cm^{-2}eV^{-1}$. Transmission electron microscopy and X-ray photoelectron spectroscopy analyses revealed that the *in situ* SiN_x layer can provide excellent passivation without causing chemical degradation to the AlN surface. These results imply the great potential of *in situ* SiN_x as an effective gate dielectric for AlN/GaN MIS devices. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4895677]

Wide bandgap III-nitrides (III-N) high electron mobility transistors (HEMTs) are excellent candidates for next-generation high-frequency power amplifiers and high-voltage power switches owing to their superior properties, such as high electron saturation velocity and large breakdown electric field.[1] In order to simultaneously achieve a high carrier density and good gate control capability, thin barriers composed of AlGaN with high Al mole fraction or even binary AlN have been studied extensively.[2–6] On the other hand, metal-insulator-semiconductor (MIS) structures are highly preferred over the Schottky-gate HEMTs due to the suppressed gate leakage current and enlarged gate swing.[3,6–18] However, the insertion of a gate dielectric creates an additional dielectric/III-N interface with high-density traps typically in the range of 10^{10}–$10^{14}\,cm^{-2}\,eV^{-1}$. These defect states can substantially deteriorate the device performances.[7–13]

Studies have shown that the interface trap states between the gate dielectric and III-N semiconductors are usually induced by exposure to air and damages in subsequent fabrication processes. These trap states are extremely sensitive to certain specific processing steps such as surface cleaning, dielectric deposition, and pre-/post-deposition treatments.[7,8] It was also found that the trap state density increases in general with Al composition in the barrier layer, probably due to native oxidation, higher surface sensitivity, or oxygen incorporation associated with high Al composition.[11,12] In particular, the trap state density of a dielectric/AlN interface can reach over $4 \times 10^{13}\,cm^{-2}eV^{-1}$ in dielectric/AlN/GaN MIS devices grown by molecular-beam epitaxy (MBE).[14,15] The situation can become even more complicated in AlN barriers grown by metalorganic chemical vapor deposition (MOCVD) since significant strain relaxation can occur in the AlN layer during temperature ramp-down. This undesirable relaxation can be minimized by adding a thin GaN cap layer on the AlN barrier.[6,16] However, the extra GaN layer between gate dielectric and AlN barrier is not preferable for a MIS device, because of the introduced additional GaN/AlN interface, the increased gate-to-channel distance and the relatively narrow bandgap of GaN. Although an *in situ* grown SiN_x by MOCVD has been reported to be the optimum passivation layer for III-nitride HEMTs,[4,17–19] interface trapping analysis for the *in situ* SiN_x MIS structures is still limited. Recently, we also demonstrated the use of SiN_x *in situ* grown by MOCVD as gate dielectrics and passivation for AlN/GaN MISHEMTs,[20,21] which show reduced gate leakage current and increased carrier concentration. To further optimize the device structure, a thorough study of the interface trapping is of great importance.

In this letter, we report on the investigation of interfacial trapping effects in SiN_x/AlN/GaN MIS structures in which the SiN_x gate dielectric was grown *in situ* by MOCVD. Double-mode capacitance-voltage (C-V) measurement and frequency dependent conductance analysis were used to evaluate the trap state densities. Remarkably, the trap state density of the MIS structure in this work is comparable to those of conventional Al_2O_3/(GaN)/AlGaN/GaN MIS devices (Refs. 9–12), and is much lower than similar AlN/GaN MIS structures capped with other dielectrics (Refs. 14,15, and 20). These results indicate the advantages of *in situ* SiN_x as gate dielectric over other *ex situ* ones. Transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) were performed to reveal the origin of the high-quality SiN_x/AlN interface.

The *in situ* SiN_x/AlN/GaN heterostructures were grown on a 2-in. sapphire substrate in an AIXTRON2000HT MOCVD system. The epi-layers consist of, from bottom to top, a 35 nm low-temperature AlN nucleation layer, a 300 nm high-temperature AlN buffer layer, a 2.7 μm undoped GaN layer, followed by a 3.5 nm AlN barrier layer and, finally, a 9 nm *in situ* SiN_x cap layer. The *in situ* SiN_x was deposited at 1145 °C immediately following the AlN/GaN heterostructure growth in the same MOCVD chamber, using silane and ammonia as precursors. Atomic force microscopy (AFM) image of the as-grown sample in Fig. 1(a) shows a smooth surface morphology. The root mean square (RMS) roughness across a 5 μm × 5 μm scanned area is 0.43 nm. Room temperature Hall measurements showed a two-dimensional electron gas (2DEG) density of $1.41 \times 10^{13}/cm^2$ with a mobility of $1010\,cm^2/V{\cdot}s$, corresponding to a sheet resistance of 438 Ω/□. The smooth surface

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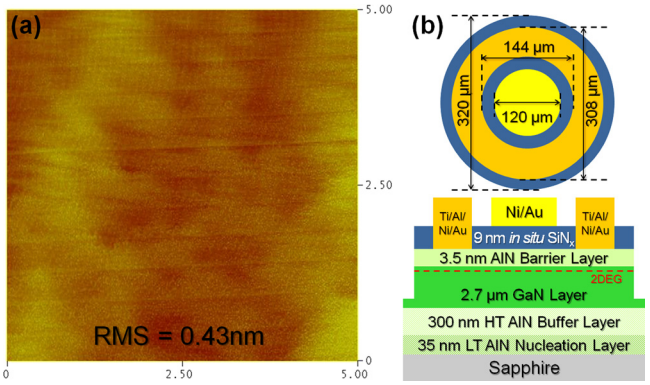

FIG. 1. (a) AFM image of the as-grown *in situ* SiN_x/AlN/GaN MISHEMT sample. (b) The architecture of the *in situ* SiN_x/AlN/GaN MIS diode.

morphology and high 2DEG mobility demonstrated that the *in situ* SiN_x cap layer effectively alleviated the relaxation of AlN barrier during the post-growth cooling process.[19] The fabrication of MIS diodes started with mesa isolation using a CF_4/O_2-based reactive ion etch (RIE), followed by a Cl_2-based inductively coupled plasma (ICP) etch. After selective removal of the SiN_x cap layer in the Ohmic contact region by RIE, Ti/Al/Ni/Au (20/150/50/80 nm) was deposited by e-beam evaporation and annealed at 850 °C for 30 s in a N_2 ambient. Finally, the Ni/Au (20/200 nm) gate metal was deposited on the *in situ* SiN_x by e-beam evaporation without any post-deposition treatments. Fig. 1(b) schematically shows the architecture of the *in situ* SiN_x/AlN/GaN MIS diode. The diameter of the circular metal gate was 120 μm.

The double-mode C-V curves of the *in situ* SiN_x/AlN/GaN MIS diode in Fig. 2 exhibit a sharp transition from depletion mode to accumulation mode, indicating a high-quality SiN_x/AlN interface. The measurements were set up with an up-and-down sweep rate of 0.05 V/s and a voltage variation of 50 mV at 100 kHz. The C-V curve in Fig. 2 shows less saturation in the accumulation region. It is an indication of barrier accumulation, where the electrons start to transfer into the barrier of the heterostructure.[11,22] As shown in the inset of Fig. 2, the clockwise hysteresis (ΔV_{th}) is as small as 25 mV when the maximum forward voltage in the sweep is at +1 V. Such hysteresis can be attributed to

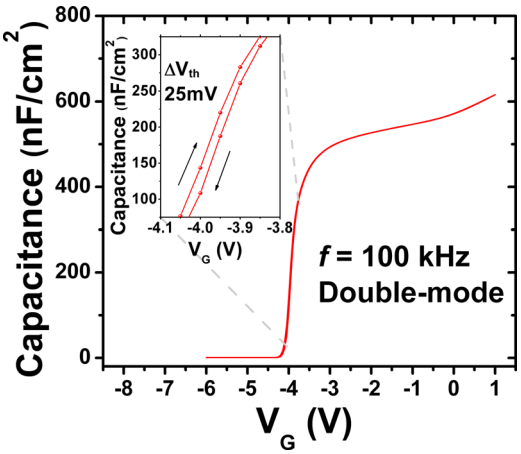

FIG. 2. Double mode C-V characteristics of the *in situ* SiN_x/AlN/GaN MIS diode. The inset shows the enlarged plot between $V_G = -4.1$ V and -3.8 V showing the hysteresis of the C-V curve.

acceptor-like states in the dielectrics or at the dielectric/barrier interfaces with a relatively long emission time constant.[9,11,22] Using

$$D_T = C_{MIS} \cdot \Delta V_{th}/e, \tag{1}$$

we estimate the density of "slow" trap states in the MIS diode to be as low as $1 \times 10^{11}\,cm^{-2}eV^{-1}$. This value is significantly lower than the reported results on Al_2O_3/(GaN)/AlGaN/GaN MIS devices.[9–11] The time constant of this "slow" trap state is larger than 100 s.

To further evaluate the interfacial trapping effects of the *in situ* SiN_x/AlN/GaN MIS structures, we performed frequency dependent conductance analysis with the frequency ranging from 1 kHz to 1 MHz. Fig. 3 shows the plot of parallel conductance (G_P/ω) as a function of the radial frequency (ω) for selected gate voltages near the threshold voltage (V_{th}) of the MIS diode. The trap state density (D_T) and the time constant (τ_T) can be extracted by fitting the experimental $G_P(\omega)$ data using[12,13,20]

$$\frac{G_p}{\omega} = \frac{qD_T}{2\omega\tau_T}\ln\left[1 + (\omega\tau_T)^2\right]. \tag{2}$$

It should be noted that the trap states measured using the frequency dependent conductance method typically exhibited short time constants in the range between 0.5 μs and 60 μs and were designated as "fast" trap states in this work.

The trap state time constant (τ_T) can be expressed by the Shockley–Read–Hall statistics

$$\tau_T = \frac{1}{v_{th}\sigma_n N_c}\exp\left(\frac{E_T}{kT}\right), \tag{3}$$

where $N_c = 4.3 \times 10^{14} \times T^{3/2}\,cm^{-3}$ is the effective density of states in the conduction band in GaN, $v_{th} = 2 \times 10^7\,cm\,s^{-1}$ is the average thermal velocity of electrons, and $\sigma_n = 1 \times 10^{-14}\,cm^2$ is the capture cross section of the trap states.[11–13,20] Thus, the trap energy level below the conduction band, designated as interfacial states (E_T), can be deduced from τ_T.

The density of "fast" trap states (D_T) as a function of their energies (E_T) for the *in situ* SiN_x/AlN/GaN MIS diode is shown in Fig. 4. The density drops sharply from about $1.85 \times 10^{12}\,cm^{-2}eV^{-1}$ at an energy of 0.32 eV to about $1.32 \times 10^{11}\,cm^{-2}eV^{-1}$ at $E_T = 0.44$ eV. These values are

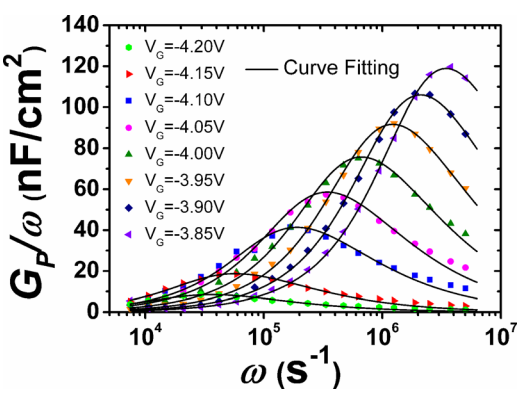

FIG. 3. Frequency dependent parallel conductance as a function of radial frequency for the MIS diode biased at selected gate voltages near V_{th}.

significantly lower, by over one order of magnitude, than the trap state densities reported on similar (GaN)/AlN/GaN MIS structures using other *ex situ* deposited gate dielectrics in Refs. 14,15, and 20. Trap state density plots for conventional (GaN)/AlGaN/GaN architecture capped with Al_2O_3 in Ref. 12 are also included in Fig. 4 for comparison. Even with a barrier composed of pure AlN, the *in situ* SiN_x-passivated MIS structure in this work exhibits a low trap state density comparable to the much more matured AlGaN/GaN MIS structures using Al_2O_3 gate dielectric. It should be noted that the previous high trap state density values for the *in situ* SiN_x/AlN/GaN MIS structure in Ref. 20 might have been stemmed from the lower quality thin barrier layer of the AlN/GaN heterostructures grown on a Si substrate. In this work, the influence of the AlN barrier quality was minimized by using sapphire substrates, with increased barrier thickness and optimized growth conditions for the heterostructure. Therefore, a fairly high quality interface was achieved.

The abruptness of the dielectric/semiconductor interface has profound impact on the trapping effects in MIS devices. Fig. 5 shows the cross sectional TEM images of the gate stack of the *in situ* SiN_x/AlN/GaN MIS sample. The images were taken near the GaN [1$\bar{1}$00] zone axis. A 9-nm-thick *in situ* SiN_x layer is observed to grow uniformly on top of AlN, as shown in Fig. 5(a). Under high magnification, one can observe that the SiN_x/AlN interface exhibits excellent abruptness without any extra interfacial layer in between (see Fig. 5(b)). This is in sharp contrast to other III-N MIS devices which usually possess a rough interface or an irregular interfacial layer.[10,23] The high-quality SiN_x/AlN interface in this work can be attributed to the *in situ* high-temperature growth of SiN_x layer. While the *in situ* process prevents the direct exposure of AlN surface to air, the high-temperature growth reduces the density of unpassivated dangling bonds on the AlN surface through enhanced surface migration of SiN_x adatoms. The smooth and abrupt interface indicates that the *in situ* SiN_x can effectively protect the AlN barrier from strain relaxation, surface oxidation and damage during the subsequent device fabrication process.

To examine the chemical composition profiles at SiN_x/AlN interface, a 300-nm AlN on sapphire sample capped with 9 nm *in situ* SiN_x was grown and probed by XPS. By sputter removal of materials from surface with argon, we

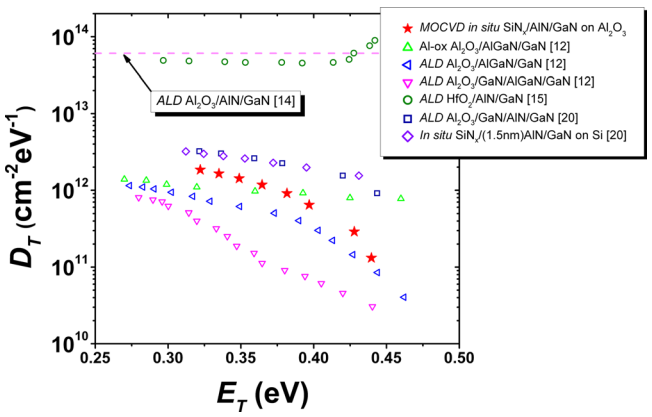

FIG. 4. Trap state density of the MIS diodes as a function of the energy level depth below the conduction band.

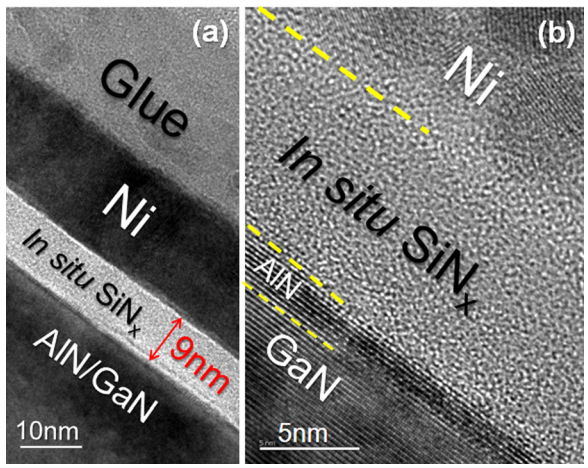

FIG. 5. Cross sectional TEM images of the gate stack showing the SiN_x/AlN/GaN architecture.

obtained a series of depth-resolved XPS spectra. Figures 6(a)–6(c) reveal the spectra at depths of around 5 nm, 8 nm, and 12 nm, respectively. The binding energy measurement at the sample surface was calibrated by correcting the adventitious C 1s peak to 285 eV. To study the bonding states of N and Al across the interface, we performed peak fitting on the N 1s and Al 2p core-level spectra. It was found that the peak distances between the Al 2p (Al-N, Al-O) and N 1s (Si-N, Al-N) remain the same for different depths, and the peak positions agree well with the reported results for SiN_x and AlN in the literature. In the N 1s spectrum taken at the SiN_x/AlN interface (i.e., ~5 and 8 nm below the surface), two components corresponding to Si-N bond and Al-N bond were identified. The Si-N peak drops significantly across the interface and finally disappears completely in the bulk AlN layer (i.e., ~12 nm below the surface). The Al 2p spectra, on the other hand, are composed of two components arising from the Al-N bond and Al-O bond at all three depths. In

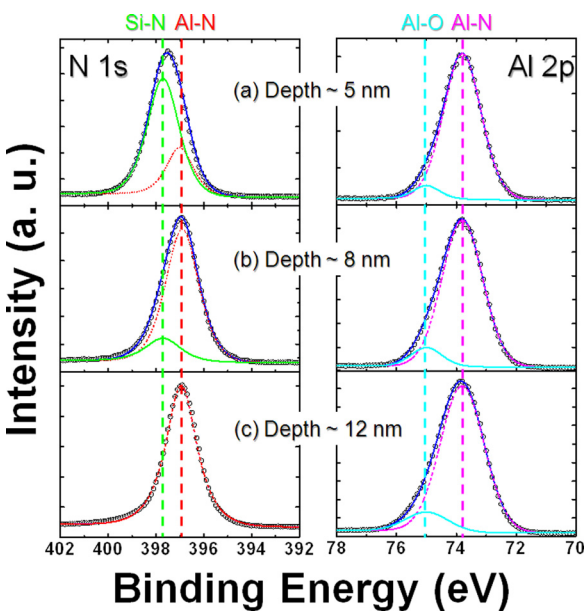

FIG. 6. N 1s and Al 2p core-level XPS spectra at three different depths from the surface.

particular, the intensities of the strong Al-N peak and weak Al-O peak remain constant at all depths. The oxygen concentrations at different depths of the *in situ* SiN_x/AlN sample are all less than 4%, while the oxygen concentration at the exposed AlN surface is as high as 15.14% for an AlN sample without any surface passivation. Therefore, the oxide-related peaks in Fig. 6 were believed to stem from the oxygen incorporation in the AlN bulk during growth rather than post-growth oxidation of the AlN surface. These results show that the *in situ* growth of SiN_x brought no obvious effects on the chemical bonding states of the AlN barrier layer. This is distinctly different from *ex situ* deposition of gate dielectrics during which exposure to air and/or plasma can induce chemical degradations including composition change, binding energy drift and formation of native oxides in the semiconductor.[10,24] Thus, the *in situ* grown SiN_x layer can indeed effectively passivate the AlN surface from oxidation and damage, leading to a high quality *in situ* SiN_x/AlN interface.

The XPS analysis also revealed that the *in situ* SiN_x in this study exhibits a N/Si ratio (1.29) closer to the ideal value of 1.33 compared with the previously reported values (1.21 and 1.25).[17,24] This can be attributed to the high temperature and NH_3 vapor pressure which promote the incorporation of N into the amorphous film. The higher N content can effectively suppress the formation of Si dangling bonds and distorted excess Si-Si bonds, leading to less midgap defect states or bulk traps. This improved stoichiometry is a key factor for the significantly reduced hysteresis in the double-mode C-V measurement and hence the remarkably low "slow" trap states density.[9,21–23]

In conclusion, we have investigated the interfacial trapping effects of AlN/GaN MIS structures with *in situ* SiN_x gate dielectric grown by MOCVD. Two dominant types of trap states, designated as "slow" and "fast" ones, were identified and characterized using double-mode C-V measurement and frequency dependent conductance analysis, respectively. Remarkably low densities of trap states have been obtained, demonstrating the feasibility of utilizing *in situ* SiN_x as gate dielectric for AlN/GaN MIS devices. The density of the "slow" trap states ($\tau_T > 100\,s$) was as low as $1 \times 10^{11}\,cm^{-2}eV^{-1}$. The density of the "fast" trap states ($0.5\,\mu s < \tau_T < 60\,\mu s$) decreased sharply from about $1.85 \times 10^{12}\,cm^{-2}eV^{-1}$ at an energy of 0.32 eV to about $1.32 \times 10^{11}\,cm^{-2}eV^{-1}$ at $E_T = 0.44\,eV$. The high quality *in situ* SiN_x/AlN interface was also examined by TEM and XPS measurements. In addition to the smooth and abrupt interface, no chemical degradation was observed at the AlN surface.

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