A Novel 700 V Monolithically Integrated Si-GaN Cascoded Field Effect Transistor

Jie Ren, *Student Member, IEEE*, Chak Wah Tang, Hao Feng, Huaxing Jiang, *Member, IEEE*, Wentao Yang, *Student Member, IEEE*, Xianda Zhou, *Member, IEEE*, Kei May Lau, *Fellow, IEEE*, and Johnny K. O. Sin, *Fellow, IEEE*

***Abstract*— In this letter, a novel monolithically integrated Si-GaN cascoded FET is designed and experimentally demonstrated for high-voltage power switching applications. The device is formed by monolithically connecting a low-voltage Si MOSFET and a high-voltage normally-on GaN MIS-HEMT on the same substrate in the cascode configuration. The interconnection distance is 50 μm which is only 2.5% of that of the conventional two-chip co-package approach (~2 mm). The fabricated cascoded FET features normally-off functionalities with a threshold voltage of 3.2 V, a drive current of 1850 A/cm^2 (630 mA/mm) at the gate bias of 15 V, a gate swing of 20 V, a specific on-resistance of 3.3 mΩ·cm^2 and a breakdown voltage of 696 V.**

***Index Terms*— Monolithic integration, cascade configuration, power FETs, GaN, MIS-HEMT, power switching electronics.**

I. Introduction

GaN-BASED power devices are promising candidates for power electronic applications due to the superior material properties of GaN compared with those of Si. But there are still obstacles keeping GaN transistors from dominating the market. The common disadvantages are the normally-on characteristics, low positive threshold voltage of Enhancement-mode devices [1], large gate leakage current, small gate voltage swing [2], and large reverse voltage drop [3]. Although some approaches were proposed to overcome one or some of the above obstacles [4], [5], it is extremely difficult to resolve these problems without sacrificing the overall performance. A hybrid Si-GaN cascode approach is the simplest solution to the above problems up to now and has been adopted by the commercial sector [6]. However, the conventional Si-GaN cascode configuration is achieved by using the two-chip co-package approach which features a long interconnection distance between the Si and GaN devices. The large interconnection parasitics induced by bonding wires will cause undesirable ringing during fast switching, resulting in lower system stability and higher switching losses [7]. One efficient way to minimize the parasitics is to fully integrate the Si MOSFET and GaN MIS-HEMT on the same substrate with a short interconnection distance. In doing so, the overall package size and assembly costs can also be reduced.

In this letter, the fabrication technology for integrating the low-voltage Si MOSFET and high-voltage GaN MIS-HEMT on the same Si substrate is developed. A Si-GaN cascoded FET is demonstrated using this technology with an interconnection distance of 50 μm which is less than 3% of that of the conventional two-chip co-package approach (~ 2 mm bonding wires).

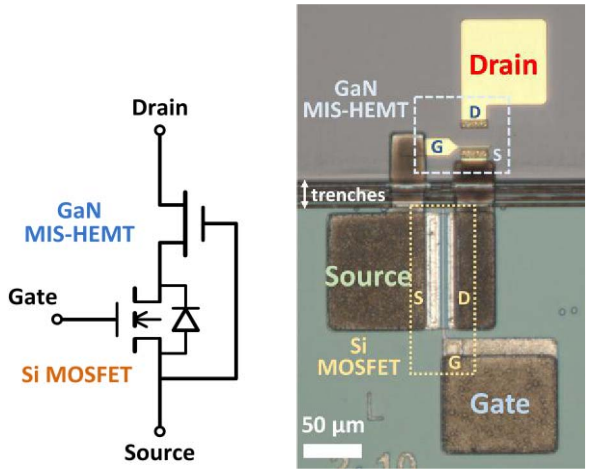

Fig. 1. (a) Circuit schematic of the cascoded FET, and (b) a top view image of the fabricated cascoded FET.

II. Device Structure and Fabrication

The schematic of the Si-GaN cascoded FET equivalent circuit is shown in Fig. 1 (a), which consists of a low-voltage normally-off Si MOSFET and a high-voltage normally-on GaN MIS-HEMT. For turning on of the cascoded FET,

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J. Ren, C. W. Tang, H. Feng, H. Jiang, W. Yang, K. M. Lau, and J. K. O. Sin are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: jrenab@connect.ust.hk).

X. Zhou is with the School of Electronics and Information Technology, Sun Yat-Sen University, Guangzhou 510006, China.

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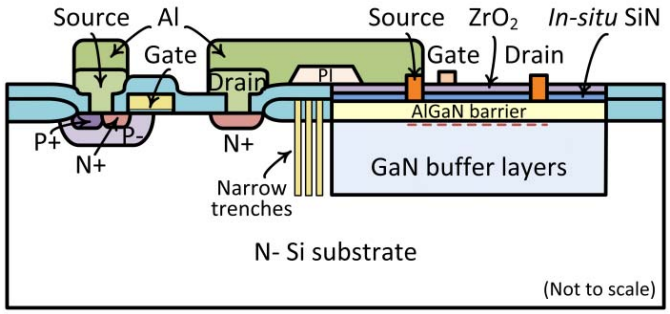

Fig. 2. Schematic cross-sectional view of the cascoded FET.

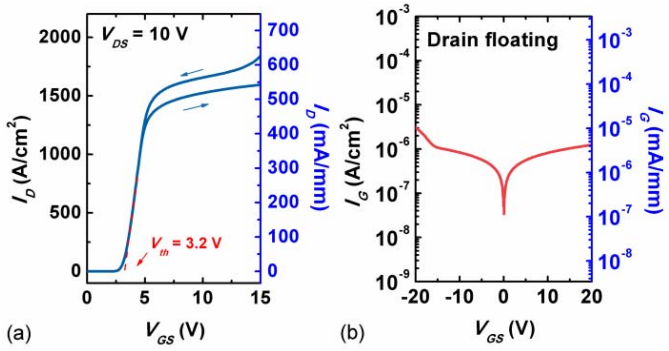

Fig. 3. (a) DC I_D-V_{GS} characteristics of the cascoded FET with the gate bias down/up sweeping at a drain bias of 10 V, and (b) DC I_G-V_{GS} characteristics of the cascoded FET with drain electrode floating.

a positive voltage is applied to the gate electrode. The drain-to-source voltage of the Si MOSFET ($V_{DS,Si}$) will then decrease, and the gate-to-source voltage of the GaN MIS-HEMT ($V_{GS,GaN}$) will increase accordingly. When $V_{GS,GaN}$ is larger than the threshold voltage of the GaN MIS-HEMT ($V_{th,GaN}$), the MIS-HEMT is turned on with high current/power capability. In the on-state, the total on-resistance is the sum of the Si MOSFET and GaN MIS-HEMT. For the device turn-off, the gate voltage is removed and the Si MOSFET is turned off with an increase in $V_{DS,Si}$ and decrease in $V_{GS,GaN}$ accordingly. When the $V_{GS,GaN}$ is lower than the $V_{th,GaN}$, the GaN MIS-HEMT is turned off with high-voltage blocking capability. During the reverse conduction, the gate and source are connected to the ground, then the body diode of the Si MOSFET and the GaN MIS-HEMT form a cascoded diode which will conduct the reverse current with a small voltage drop [8].

A top view image of the fabricated cascoded FET is shown in Fig. 1 (b). It can be seen that the Si and GaN devices are placed on the same substrate with a distance of 50 μm. Cross-sectional view of the cascoded FET is shown in Fig. 2. The monolithic integration technology used for the cascoded FET fabrication is from the continued development of the cascoded diode [8]. The process begins with a 4-inch n- Si (111) wafer. The Si devices are isolated by LOCOS. Besides, the Si and GaN device regions are isolated by etched narrow trenches. Then the approximately 4 μm AlGaN/GaN epitaxial layers with 8 nm *in-situ* SiN are grown in the Si recessed windows by MOCVD selective epitaxial growth (SEG). A near planar configuration of the GaN and Si device surface is achieved, which is important for fine-pattern lithography. Subsequently, the Si laterally diffused MOSFET processes are carried out, including poly Si gate etching and junction formation. During the high-temperature drive-in step of the p-body region, SiO_2 is used to cover the GaN epitaxial layers to protect the surface form decomposition [9]. After that, the GaN MIS-HEMT is processed with argon implantation isolation. And the *in-situ* SiN and 19 nm of ALD ZrO_2 are used as the gate dielectrics [10]. Finally, the Si and GaN devices are connected by Al metal lines.

III. Experimental Results and Discussion

In the fabricated cascoded FET, the active area of the Si MOSFET is 300 μm^2, where the poly Si gate length, gate-to-drain distance and gate width are 2 μm, 1 μm and 100 μm, respectively. The active area of the GaN MIS-HEMT is 380 μm^2, with a gate length of 2 μm, gate-to-source distance of 2 μm, gate-to-drain distance ($L_{GD,GaN}$) of 15 μm, and gate width of 20 μm. The interconnection distance between the Si MOSFET and GaN MIS-HEMT is 50 μm.

Fig. 3 (a) shows the dc transfer characteristics of the Si-GaN cascoded FET, which have been normalized to the total active area (680 μm^2, the sum of the active area of the Si MOSFET and the GaN MIS-HEMT), and the gate width of the MIS-HEMT (W_{GaN}, 20 μm) as represented by the left axis and right axis, respectively. The V_{th} determined by the linear extrapolation method is extracted to be 3.2 V. Furthermore, as shown in Fig. 3 (b), a large gate swing of 20 V is measured. At the V_{GS} of $\pm$ 20 V, the gate leakage current is smaller than 10^{-5} mA/mm, which is difficult to achieve in GaN-based transistors. Such a high V_{th} and large gate swing are important for preventing the faulty turn-on by electromagnetic interference and make the cascoded FET compatible with the existing gate drive circuits designed for Si-based power transistors [11]. The current on/off ratio is measured to be 2×10^8. The transfer curve is obtained using double sweeping mode at V_{DS} of 10 V, and no V_{th} shift is observed when the V_{GS} sweeps from 15 V down to 0 V and from 0 V up to 15 V. It indicates a very good interface quality of the Si MOSFET. The double sweep I_D-V_{GS} characteristics show approximately 10 % discrepancy in I_D at V_{GS} larger than 5 V. This is due to the unoptimized surface passivation of the GaN MIS-HEMT, which can be further improved by combining additional PECVD SiN passivation [12].

The dc output characteristics of the cascoded FET are shown in Fig. 4. The dc specific on-resistance ($R_{on,sp}$) is extracted as 3.3 m$\Omega \cdot$ cm^2 (on-resistance normalized to total active area), and 9.7 $\Omega \cdot$ mm (on-resistance normalized to W_{GaN}) at a gate bias of 15 V. The device exhibits a drive current of 1850 A/cm^2 (normalized to total active area) and 630 mA/mm (normalized to W_{GaN}). In the saturation region of the output curve with the gate bias of 15 V, the $V_{GS,GaN}$ is measured to be -1.5 V. The GaN MIS-HEMT with $V_{th,GaN}$ of -7 V has a gate overdrive voltage of 5.5 V. This ensures the higher drive current (630 mA/mm) of the cascoded FET compared with the normally-off GaN FETs [1]–[5], [13].

During the off-state breakdown test, the gate and source electrodes are grounded with the substrate floating.

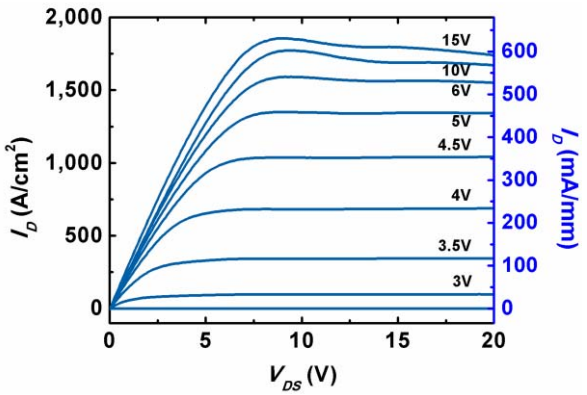

Fig. 4. DC I_D-V_D characteristics of the cascoded FET.

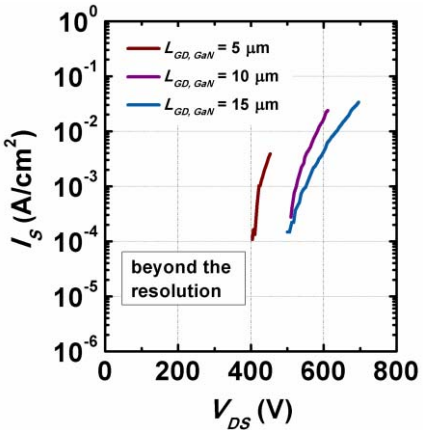

Fig. 5. Off-state I-V characteristics of the fabricated cascoded FETs with various $L_{GD,GaN}$.

When V_{DS} increases, the Si MOSFET is driven into avalanche breakdown due to the high leakage current from the source of the GaN MIS-HEMT. The cascoded FET continues blocking the increased reverse voltage by the GaN MIS-HEMT with the Si MOSFET in avalanche mode. A resistor or a Zener diode in parallel with the Si MOSFET can improved the device reliability in the off-state [14]. Due to the good leakage suppression of the Si MOS gate structure, the gate current of the cascoded FET is negligible compared with the source and drain leakage current. The off-state source current of the cascoded FETs with various GaN MIS-HEMTs dimensions are measured by Tektronix 370A and plotted in Fig. 5. V_{BD} of the cascoded FETs with $L_{GD,GaN}$ of 5 μm, 10 μm, and 15 μm are 453 V, 611 V and 696 V, respectively. For the device with $L_{GD,GaN}$ of 15 μm, the source leakage current is 0.034 A/cm^2 at the breakdown point, which is equal to 0.01 mA/mm when normalized to W_{GaN}. At 500 V, the source leakage current is approximately 0.1 mA/cm^2 (0.03 μ A/mm), which is comparable with the state-of-art normally-off GaN-based MIS (MOS)-HEMTs [5], [13].

IV. Conclusion

In conclusion, a Si-GaN cascoded FET has been demonstrated using the monolithic integration technology. The device features an on-chip interconnection distance of 50 μm, a threshold voltage of 3.2 V, a gate swing of 20 V, a specific on-resistance of 3.3 m$\Omega \cdot$ cm^2 and a breakdown voltage of 696 V. Furthermore, the technology provides the foundation to explore the fully integration of III-Nitride compound semiconductor devices/circuits with Si devices/circuits for power electronic applications.

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