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To cite this article: Yaoqiao Hu *et al* 2018 *Semicond. Sci. Technol.* **33** 045004

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# Chemical vapor deposited monolayer MoS<sub>2</sub> top-gate MOSFET with atomic-layer-deposited ZrO<sub>2</sub> as gate dielectric

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Received 15 September 2017, revised 8 December 2017

Accepted for publication 24 January 2018

Published 6 March 2018



## Abstract

For the first time, ZrO<sub>2</sub> dielectric deposition on pristine monolayer MoS<sub>2</sub> by atomic layer deposition (ALD) is demonstrated and ZrO<sub>2</sub>/MoS<sub>2</sub> top-gate MOSFETs have been fabricated. ALD ZrO<sub>2</sub> overcoat, like other high-*k* oxides such as HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub>, was shown to enhance the MoS<sub>2</sub> channel mobility. As a result, an on/off current ratio of over 10<sup>7</sup>, a subthreshold slope of 276 mV dec<sup>-1</sup>, and a field-effect electron mobility of 12.1 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> have been achieved. The maximum drain current of the MOSFET with a top-gate length of 4 μm and a source/drain spacing of 9 μm is measured to be 1.4 μA μm<sup>-1</sup> at V<sub>DS</sub> = 5 V. The gate leakage current is below 10<sup>-2</sup> A cm<sup>-2</sup> under a gate bias of 10 V. A high dielectric breakdown field of 4.9 MV cm<sup>-1</sup> is obtained. Gate hysteresis and frequency-dependent capacitance–voltage measurements were also performed to characterize the ZrO<sub>2</sub>/MoS<sub>2</sub> interface quality, which yielded an interface state density of ~3 × 10<sup>12</sup> cm<sup>-2</sup> eV<sup>-1</sup>.

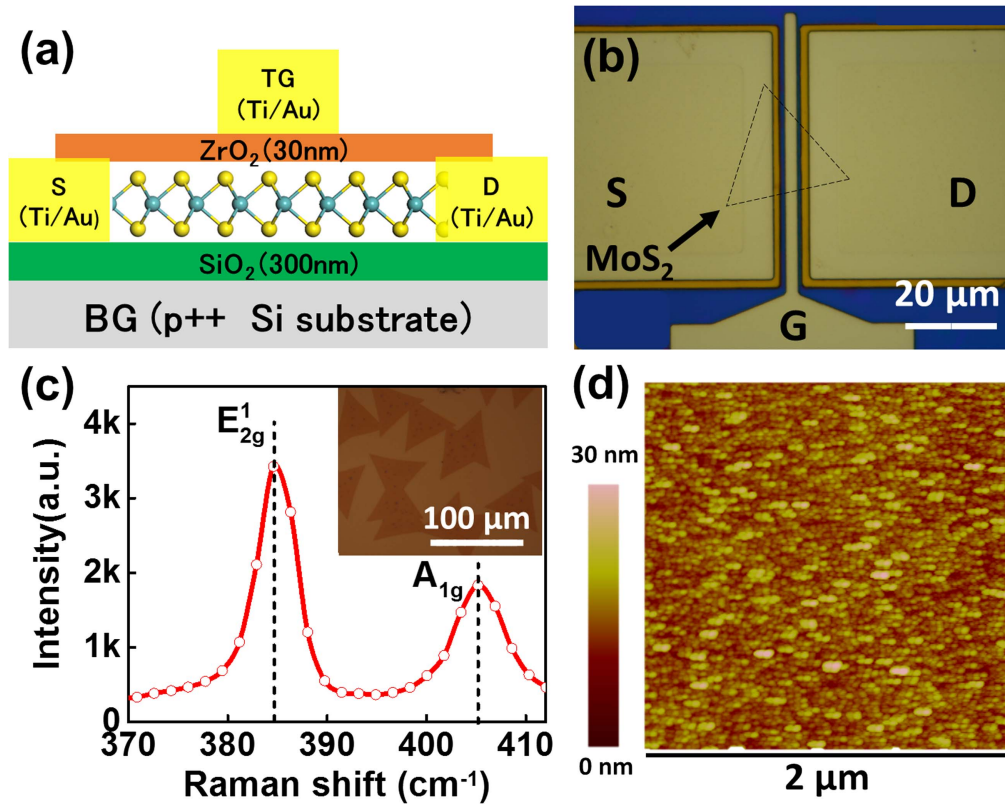
Keywords: atomic layer deposition, ZrO<sub>2</sub>, MoS<sub>2</sub>, top-gate transistor

(Some figures may appear in colour only in the online journal)

## 1. Introduction

With a sizable bandgap that changes from indirect to direct in single layers, semiconducting two-dimensional molybdenum disulfide (MoS<sub>2</sub>) has recently gained tremendous interest for transistors, photodetectors and electroluminescent devices [1–3]. Thanks to the enhanced electrostatic control of the gate over the channel [2–4], MoS<sub>2</sub> field effect transistors (FETs) have demonstrated outstanding device performance, such as high on/off current ratios up to 10<sup>8</sup> [2, 3], a near-ideal subthreshold swing of 60 mV dec<sup>-1</sup> [3, 4], and good carrier mobilities [5]. To increase the gate capacitance and preserve a high channel mobility through the dielectric screening effect [6], integration of high-*k* technology with MoS<sub>2</sub> transistors is essential. However, atomic-layer deposition (ALD) of high-quality gate dielectrics on 2D materials has proven challenging [7–10] because of the lack of surface-dangling bonds.

The high-*k* dielectrics investigated to date include TiO<sub>2</sub>, SrTiO<sub>3</sub>, Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, ZrO<sub>2</sub>, and the associated silicates [11–15]. Among these, Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, and ZrO<sub>2</sub> have been widely studied and are believed to be the most promising candidates due to their high dielectric constant, good thermodynamic stability, and reasonable band gap [16, 17]. Although Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> have been intensely used to fabricate MoS<sub>2</sub> top-gate transistor [18, 19], ZrO<sub>2</sub> is, to the best of our knowledge, only reported in back-gate transistors [20]. By transferring MoS<sub>2</sub> flakes onto a pre-deposited high-*k* dielectric layer, the back-gate approach bypasses the challenges associated with ALD deposition on 2D materials. However, there would remain significant interest in readily using the chemical vapor deposition (CVD) grown MoS<sub>2</sub> films to build top gate transistors which are more in line with mainstream transistor design and integration.



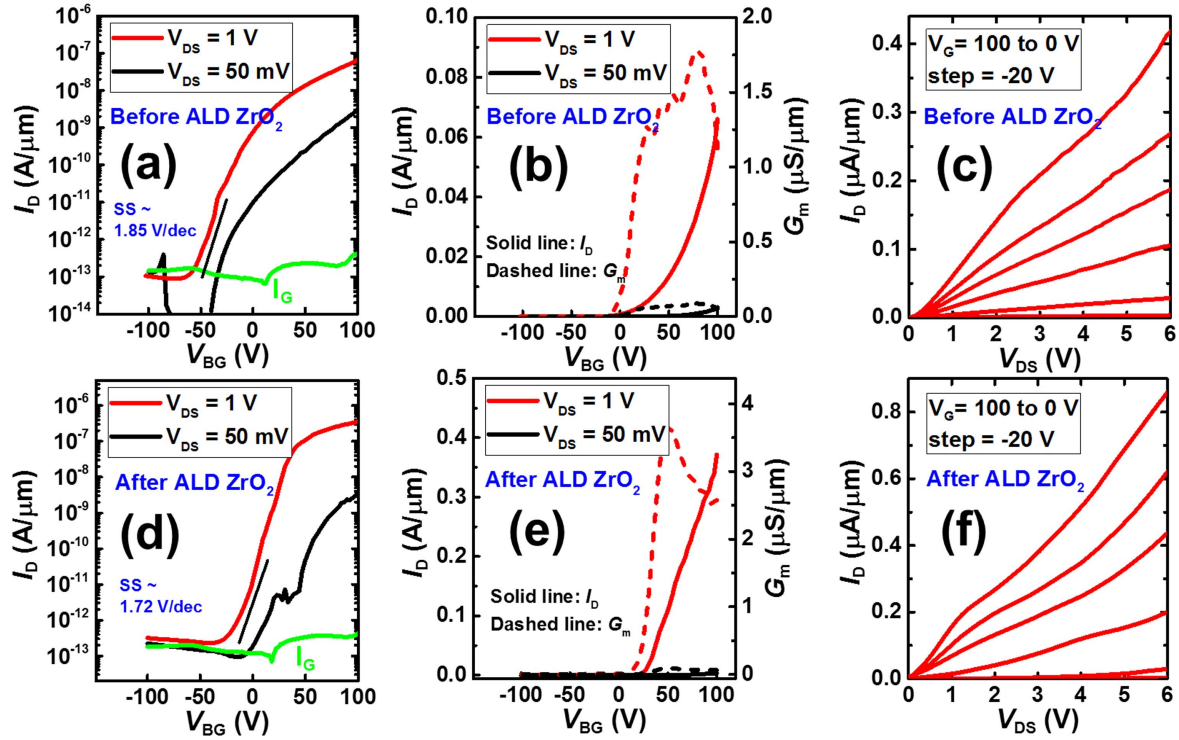
**Figure 1.** (a) Schematic illustration of a monolayer  $\text{ZrO}_2/\text{MoS}_2$  top-gate field-effect transistor. The p++ Si substrate acts as global back gate (BG) while Ti/Au metal stack as top gate (TG). (b) Optical microscope image of a typical  $\text{MoS}_2$  device. (c) Raman spectrum of the as-grown  $\text{MoS}_2$  film on Si/SiO<sub>2</sub> substrate measured at room temperature. Laser wavelength for Raman measurement is 514 nm. The inset shows the optical image of monolayer  $\text{MoS}_2$  on SiO<sub>2</sub>/Si substrate. (d) AFM image of the ALD- $\text{ZrO}_2$  on  $\text{MoS}_2$ .

Previous studies on high- $k/\text{MoS}_2$  based top-gated transistors have almost exclusively been focused on mechanically exfoliated flakes. However, due to the small size of few-layer films and possible extraneous contamination from exfoliation process, mechanical exfoliation is not a scalable or reproducible method for commercial use [21]. New synthetic routes such as CVD allow for both high-quality and large-area thin films. In fact, a variety of 2D materials including graphene [22], boron nitride [23] and  $\text{MoS}_2$  [24] have reportedly been synthesized by CVD methods. However, the electrical properties of CVD  $\text{MoS}_2$ , especially the device performances of top-gated transistors, have not been comprehensively studied.

In this work, we report the first realization of CVD monolayer  $\text{MoS}_2$  top-gate transistors with ALD  $\text{ZrO}_2$  as gate dielectric. Using a low-temperature ALD process, we achieve direct deposition of  $\text{ZrO}_2$  on pristine monolayer  $\text{MoS}_2$ . The fabricated top-gate transistors exhibit well-behaved characteristics with high on/off current ratios and low gate leakage current. The influence of ALD  $\text{ZrO}_2$  on the electrical performance of  $\text{MoS}_2/\text{SiO}_2$  back-gate transistor is discussed. The dielectric properties, as well as the  $\text{MoS}_2/\text{ZrO}_2$  interface quality have been investigated.

## 2. Experimental details

Figure 1(a) displays a cross-section schematic of the  $\text{MoS}_2$  MOSFET with a top-gate electrode. A top-view optical microscope image of a fabricated device is shown figure 1(b). Monolayer  $\text{MoS}_2$  reported in this work were grown by CVD on a heavily doped Si substrate capped with 300 nm SiO<sub>2</sub>. High purity  $\text{MoO}_3$  and S powder were used as precursors. The as-grown single-crystal [25] triangular shaped  $\text{MoS}_2$  (with average edge length  $\sim 40 \mu\text{m}$ ) was characterized by Raman scattering. As shown by the Raman spectrum in figure 1(c), the frequency difference between the in-plane ( $E'_{2g}$ ,  $\sim 385.1 \text{ cm}^{-1}$ ) and out-of-plane ( $A_{1g}$ ,  $\sim 405.1 \text{ cm}^{-1}$ ) phonon modes confirms that the deposited  $\text{MoS}_2$  is of monolayer thickness [26]. The device fabrication started with deposition of source/drain (S/D) electrodes (10/90 nm Ti/Au) by standard lithographic patterning.  $\text{ZrO}_2$  was then deposited directly on the  $\text{MoS}_2$  films in an Oxford OpAL ALD reactor at a temperature of 200 °C. Tetrakis ethylmethylamino zirconium (TEMAZ) and water were used as precursors. After 300 ALD cycles,  $\sim 27 \text{ nm}$   $\text{ZrO}_2$  was deposited and confirmed by ellipsometry measurement. Subsequently, S/D contact holes were opened using a combination of dry and wet etching of the  $\text{ZrO}_2$  layer. Finally, gate metal (10/90 nm Ti/Au) was defined. A dimension 3100 AFM system was used to examine the surface morphology after ALD deposition. All electrical tests were carried out



**Figure 2.** Transfer characteristics of MoS<sub>2</sub>/SiO<sub>2</sub> back-gate transistor in log scale (a), (d) and linear scale (b), (e); output characteristics (c), (f) for the same ( $L = 4 \mu\text{m}$ ,  $W = 12 \mu\text{m}$ ) device before (a)–(c) and after (d)–(f) the deposition of a 27 nm ALD ZrO<sub>2</sub> overcoat.

using an Agilent 4156C precision semiconductor parameter analyzer at room temperature.

### 3. Results and discussion

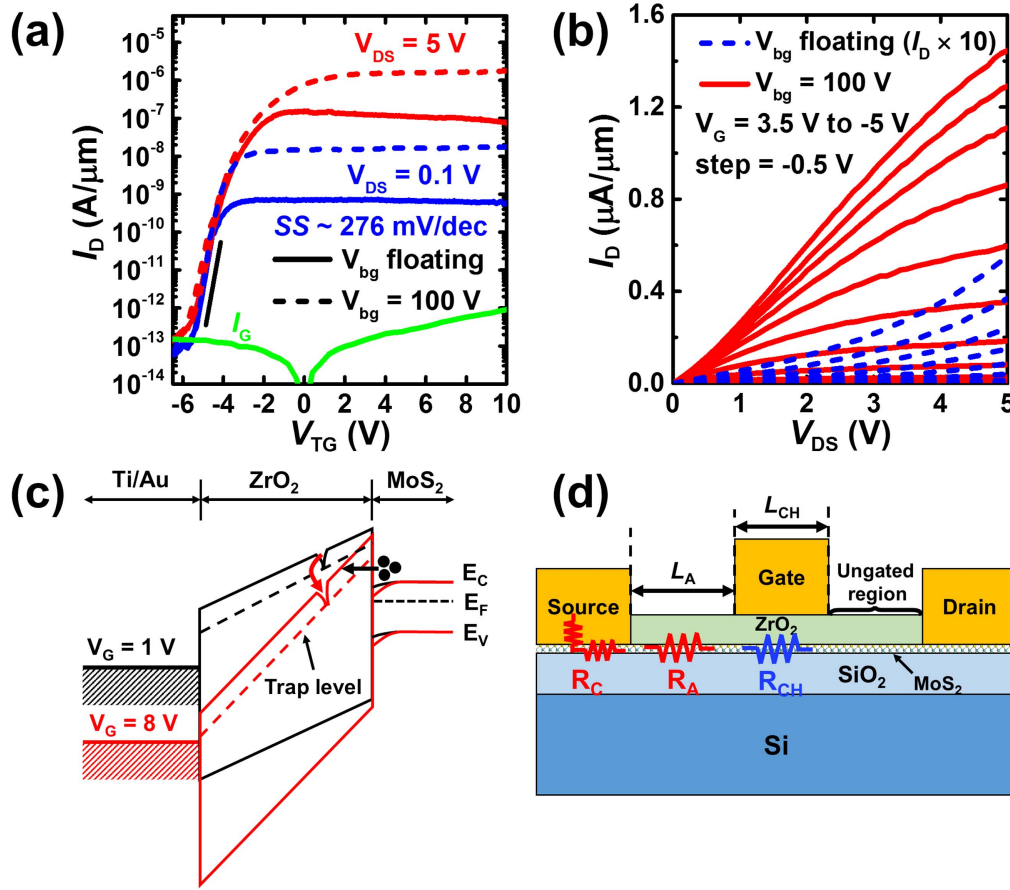
Figure 1(d) shows a representative AFM image of the surface of the atomic-layer-deposited ZrO<sub>2</sub> on single-layer MoS<sub>2</sub>. The ZrO<sub>2</sub> is continuous but exhibits island type morphology [27]. A root mean square roughness of 2.95 nm was obtained across a scanning area of  $2 \times 2 \mu\text{m}^2$ . This surface roughness is inferior when compared with the optimized ALD deposition of Al<sub>2</sub>O<sub>3</sub> on MoS<sub>2</sub> (0.58 nm in rms for Al<sub>2</sub>O<sub>3</sub> on MoS<sub>2</sub> [28]) and needs to be further optimized. The roughness could undermine the mobility of MoS<sub>2</sub> underneath and cause gate leakage fluctuations. Nevertheless, microscope observations indicated a complete coverage of direct ALD on pristine MoS<sub>2</sub>, which is attributed to physical absorption of precursors on the basal plane. This is also observed in previous demonstrations of ALD Al<sub>2</sub>O<sub>3</sub> [10] and HfO<sub>2</sub> [27] on MoS<sub>2</sub> at the optimized temperature window.

We first discuss the influence of ALD ZrO<sub>2</sub> overcoat on the electrical performance of CVD monolayer MoS<sub>2</sub>/SiO<sub>2</sub> back-gate transistor. Figure 2 shows the transfer and output characteristics of a ZrO<sub>2</sub>/SiO<sub>2</sub> back-gate FET before and after the deposition of ZrO<sub>2</sub>. Previous studies have shown that high- $k$  oxides HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> encapsulation can greatly improve the MoS<sub>2</sub> channel mobility through Coulomb scattering screening effect [6]. In our case, the device shows more than doubled drive current after ZrO<sub>2</sub> deposition, implying mobility improved by ZrO<sub>2</sub> overcoating which is similar to

HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub>. The field-effect mobility is extracted from the  $I_D$  versus  $V_{bg}$  curves in the linear region by using the expression  $\mu = L/V_{DS}C_{ox} \times (dI_{DS}/dV_{bg})$ , where  $L$  and  $W$  are the channel length and width,  $V_{DS}$  is the source–drain voltage, and  $C_{ox}$  is the back-gate capacitance per unit area. At room temperature, the extracted mobility before and after ZrO<sub>2</sub> top dielectric are  $6.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $11.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , respectively. We attribute the mobility enhancement to the suppressed charged impurity scattering, which is similar to the Al<sub>2</sub>O<sub>3</sub>/MoS<sub>2</sub> and HfO<sub>2</sub>/MoS<sub>2</sub> top-gate transistors [6, 18]. The mobility with ZrO<sub>2</sub> overcoating is not as high as that of the best transistor using HfO<sub>2</sub> [7] as the gate dielectric, which is possibly attributed to the large Coulomb scattering from fixed charges near the ZrO<sub>2</sub> surface induced by the comparatively lower ALD deposition temperature [29]. In addition, we observe that while our device was intrinsically n-doped (a negative bias voltage required to reach neutral point) for both before and after ALD growth, the threshold voltage was positively shifted after the ZrO<sub>2</sub> deposition. The reason for this shift is not clear and is still under investigation.

Figures 3(a) and (b) show the transfer and output characteristics of a ZrO<sub>2</sub>/MoS<sub>2</sub> top-gate FET respectively. With the back-gate (heavily doped p++ Si substrate) floating, the device shows typical n-type conduction behavior and an on/off current ratio of  $\sim 10^6$ . At  $V_{DS} = 5$  V, the subthreshold slope (SS) is 276 mV per decade. The relatively large SS can be attributed to the un-optimized MoS<sub>2</sub>/ZrO<sub>2</sub> interface. Furthermore, with  $V_{DS} = 5$  V and back gate floating, we note clear reduction of drain current when top-gate voltage is increased. We speculate this is likely due to the injection and trapping of electrons inside the gate dielectric (figure 3(c)).





**Figure 3.** (a) Transfer characteristics of  $\text{ZrO}_2/\text{MoS}_2$  top-gate transistor ( $L = 4 \mu\text{m}$ ,  $W = 12 \mu\text{m}$ ) and (b) output characteristics of device indicated in (a). For clarity, the drain current with back-gate floating is multiplied by 10 times. (c) Schematic band diagram of  $\text{Ti}/\text{ZrO}_2/\text{MoS}_2$  MOS structure at  $V_{\text{TG}} = 1 \text{ V}$  and  $V_{\text{TG}} = 8 \text{ V}$ . With a high top gate voltage, electron injection and trapping would occur due to the reduced tunneling barrier. (d) Schematic illustration of access resistance and contact resistance in a gate-underlap  $\text{MoS}_2$  transistor.  $R_{\text{C}}$ : contact resistance,  $R_{\text{A}}$ : access resistance,  $R_{\text{CH}}$ : channel resistance,  $L_{\text{A}}$ : access region length.

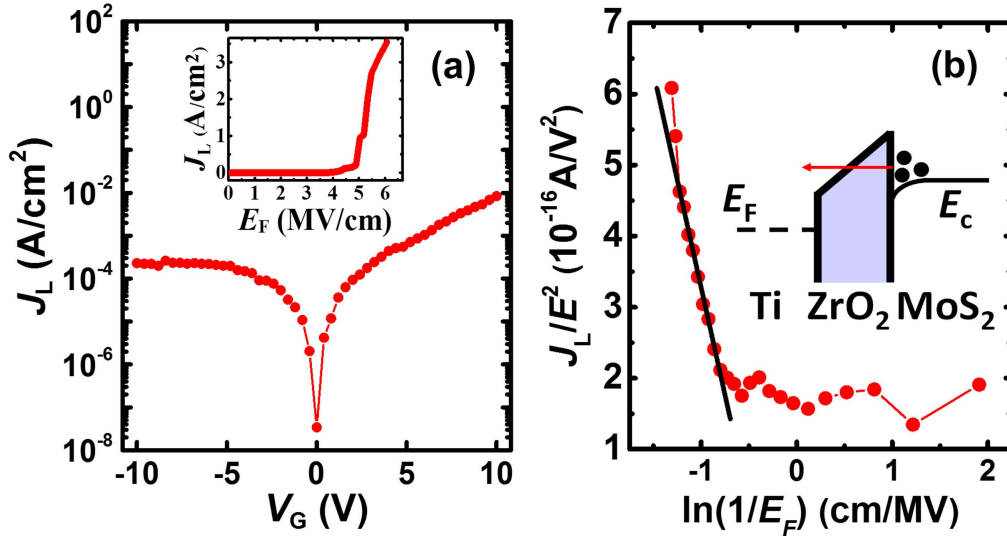
**Table 1.** The comparison of some key device parameters between different CVD monolayer  $\text{MoS}_2$  top-gate MOSFETs.

| Dielectrics       | $\text{Al}_2\text{O}_3$                              | $\text{HfO}_2$                                       | $\text{ZrO}_2$ (this work)                         |
|-------------------|------------------------------------------------------|------------------------------------------------------|----------------------------------------------------|
| On/off            | $10^7$ [19]                                          | $10^8$ [35]                                          | $10^7$                                             |
| Off state leakage | $10^{-7} \mu\text{A} \mu\text{m}^{-1}$ [19]          | $10^{-7} \mu\text{A} \mu\text{m}^{-1}$ [32]          | $10^{-7} \mu\text{A} \mu\text{m}^{-1}$             |
| Mobility          | $24 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [19] | $55 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [33] | $12 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$    |
| Drive current     | $1.0 \mu\text{A} \mu\text{m}^{-1}$ [19]              | $55 \mu\text{A} \mu\text{m}^{-1}$ [19]               | $1.4 \mu\text{A} \mu\text{m}^{-1}$                 |
| $G_{\text{m}}$    | —                                                    | $38 \mu\text{S} \mu\text{m}^{-1}$ [19]               | $2.23 \mu\text{S} \mu\text{m}^{-1}$                |
| SS                | $140 \text{ mV dec}^{-1}$ [31]                       | $110 \text{ mV dec}^{-1}$ [32]                       | $276 \text{ mV dec}^{-1}$                          |
| $D_{\text{it}}$   | $<10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ [34]      | —                                                    | $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ |

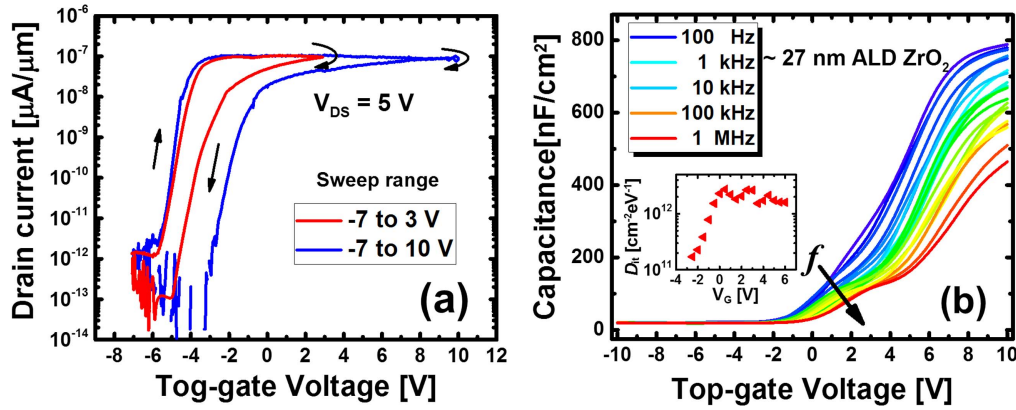
When the top gate is biased at lower voltage, electron injection from the channel to the  $\text{ZrO}_2$  dielectric is suppressed by the large tunneling barrier. With increased  $V_{\text{TG}}$ , this process would be greatly enhanced since the tunneling barrier is reduced. If a large proportion of electrons are trapped, the current is then reduced.

The  $\text{ZrO}_2/\text{MoS}_2$  top-gate transistors in this work are gate-underlap transistors with large S/D access regions (figure 3(d)). Previous studies have found that the un-gated channel regions can lead to significant access resistance and contact resistance, thus obscuring the intrinsic performances of the top-gate  $\text{MoS}_2$  transistors [30]. To minimize such

influence and obtain the intrinsic device parameters, devices are also characterized under a large positive back-gate voltage. The positive back-gate voltage induces electron accumulation within S/D access region and thus reduce the access resistance and contact resistance. From figure 3(a), when a back-gate voltage of 100 V was applied, drive current was enhanced by 20 times, leading to a greater on/off current ratio of over  $10^7$ . The current enhancement is also shown in output characteristics in figure 3(b), where the on-state resistance was significantly improved under a positive back-gate bias. Consequently, the maximum drive current reached  $\sim 1.4 \mu\text{A} \mu\text{m}^{-1}$  at  $V_{\text{DS}} = 5 \text{ V}$  and  $V_{\text{G}} = 3.5 \text{ V}$ . The extracted



**Figure 4.** (a) Leakage current characteristics of a MOSFET structure (Ti/ALD-ZrO<sub>2</sub>/MoS<sub>2</sub>). The inset of the figure shows the breakdown field of 27 nm ALD ZrO<sub>2</sub> on MoS<sub>2</sub>. (b) A  $J_L/E^2$  versus  $\ln(1/E_F)$  plot for the positive biasing condition, consistent with Fowler–Nordheim tunneling behavior.



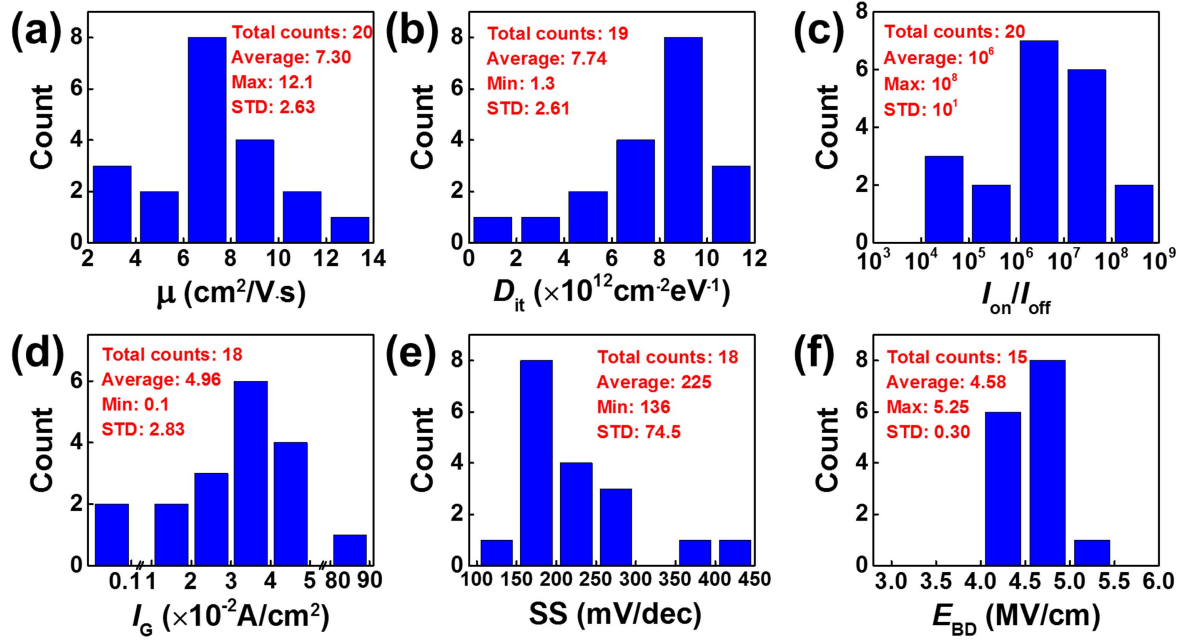
**Figure 5.** (a) Gate hysteresis behavior of the demonstrated device with two different gate sweep ranges. (b) Frequency-dependent  $C$ – $V$  characteristics of the MOSFET device measured at room temperature. The inset shows the interface state distribution determined using the high-low frequency method.

mobility with the back-gate biased at 100 V is  $12.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which is close to the value determined from back-gate transistor. Table 1 summarizes the device parameters from CVD monolayer MoS<sub>2</sub> MOSFETs using different high- $k$  oxides as top-gate dielectrics.

To study the electrical properties of the ZrO<sub>2</sub>/MoS<sub>2</sub> gate stack, gate leakage current was measured at both bias polarities in our top-gate transistor. A bias was applied to the gate terminal, with both the drain and source grounded. As shown in figure 4(a), the gate leakage current density  $J_L$  falls in the range  $10^{-4}$ – $10^{-2} \text{ A cm}^{-2}$  under gate biases below 10 V, which is considerably lower than that of direct ALD deposited HfO<sub>2</sub>(28 nm)/MoS<sub>2</sub> gate stack [35]. The inset of figure 4(a) plots the  $J_L$  as a function of the electric field  $E_F$ . The breakdown field ( $E_{BD}$ ) for 27 nm ALD ZrO<sub>2</sub> on MoS<sub>2</sub> is calculated to be  $4.9 \text{ MV cm}^{-1}$ , comparable to the value of ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> bilayer reported in the literature [36]. Figure 4(b) plots the  $J_L$ – $E_F$  curve at positive gate biases. With  $\ln(1/E_F) < -0.8$  ( $V_G > 6 \text{ V}$ ), electron injection from MoS<sub>2</sub> follows the

Fowler–Nordheim tunneling rule, as evidenced by the linear  $J_L/E_F^2$  versus  $\ln(1/E_F)$  relationship. The low leakage current and high breakdown field suggest good dielectric properties of ALD ZrO<sub>2</sub> on MoS<sub>2</sub>.

Gate hysteresis and frequency-dependent capacitance–voltage ( $C$ – $V$ ) have been measured to investigate the interface quality between ZrO<sub>2</sub> and MoS<sub>2</sub>. In figure 5(a), the gate is swept from negative to positive then back to negative voltage, with the back gate floating. The hysteresis becomes more pronounced when the sweep range is increased. This behavior, together with larger hysteresis gap at higher gate voltage, suggests a higher interface trap state density near the conduction band since the larger gate voltage, the closer the fermi level is to the conduction band. In figure 5(b), the  $C$ – $V$  curve shows typical n-type MOS capacitor behavior, with a clear transition from depletion to accumulation when the gate voltage increases. The gate oxide capacitance  $C_{ox}$  was determined to be  $790 \text{ nF cm}^{-2}$  from the maximum capacitance at 100 Hz, which corresponded to an EOT of 4.4 nm. A



**Figure 6.** Statistical studies on electrical properties of (a) mobility, (b) interface state density, (c) on/off current ratio, (d) gate leakage, (e) subthreshold slope, and (f) dielectric breakdown field for ZrO<sub>2</sub>/MoS<sub>2</sub> top-gate transistors.

larger frequency dispersion was observed at the accumulation region, which also indicates a high interface trap state density close to the conduction band. We further quantitatively extracted the interface state density using the high-low frequency method which gives the formula [37]:

$$D_{it}(V_G) = \frac{C_{ox}}{q} \left( \frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right), \quad (1)$$

where  $V_G$ ,  $D_{it}$ ,  $q$ ,  $C_{lf}$ , and  $C_{hf}$  represent gate voltage, interface state density, the elementary charge, low-frequency capacitance, and high-frequency capacitance, respectively. The inset to figure 5(b) plots the calculated  $D_{it}$  versus gate voltage in the transition region of the CV curve (from accumulation to depletion). The  $D_{it}$  is approximately  $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ . To reduce the gate hysteresis and interface states, further studies should focus on the chemical absorption process during the ALD growth and the improvement of high- $k$ /MoS<sub>2</sub> interface quality.

Further, in view of device-to-device variation, a statistical study of the key device parameters is performed to gain a comprehensive understanding of the electrical performances. The data are presented in figure 6. A total of 20 devices are studied with different channel lengths and widths. The average values and standard deviations are analyzed. These figures show a broad distribution of different electrical parameters which can be connected to the nonuniformity of synthesized MoS<sub>2</sub> film and fabrication process. The large fluctuations of gate leakage also suggest nonuniform thickness of ZrO<sub>2</sub> which has been discussed in the previous part.

#### 4. Conclusion

In summary, we have experimentally demonstrated top-gate MOSFETs with monolayer MoS<sub>2</sub> channel and ALD ZrO<sub>2</sub> as gate dielectric. AFM and  $I$ - $V$  studies show that ALD ZrO<sub>2</sub> can be directly deposited on MoS<sub>2</sub> with low leakage current and high breakdown field. ZrO<sub>2</sub> overlayer can improve the MoS<sub>2</sub> channel mobility. Gate hysteresis and  $C$ - $V$  measurements reveal a ZrO<sub>2</sub>/MoS<sub>2</sub> interface state density of about  $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ . These results suggest that ALD ZrO<sub>2</sub> could be a promising candidate for gate dielectric application in MoS<sub>2</sub>-based MOSFETs.

#### Acknowledgments

This work was supported by Grant (No. 16230916) from the Research Grants Council of Hong Kong and an Initiation Grant (IGN15EG01) from HKUST. The authors would like to thank the NFF and MCPF of HKUST for technical support. Helpful discussions with L Y Wang and B Lai are also appreciated.

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#### References

- [1] Wang Q H, Kalantar-Zadeh K, Kis A, Coleman J N and Strano M S 2012 Electronics and optoelectronics of two-

- dimensional transition metal dichalcogenides *Nat. Nanotechnol.* **7** 699–712
- [2] Radisavljevic B, Radenovic A, Brivio J, Giacometti I V and Kis A 2011 Single-layer MoS<sub>2</sub> transistors *Nat. Nanotechnol.* **6** 147–50
  - [3] Yoon Y, Ganapathi K and Salahuddin S 2011 How good can monolayer MoS<sub>2</sub> transistors be? *Nano Lett.* **11** 3768–73
  - [4] Das S, Chen H Y, Penumatcha A V and Appenzeller J 2012 High performance multilayer MoS<sub>2</sub> transistors with scandium contacts *Nano Lett.* **13** 100–5
  - [5] Kim S et al 2012 High-mobility and low-power thin-film transistors based on multilayer MoS<sub>2</sub> crystals *Nat. Commun.* **3** 1011
  - [6] Radisavljevic B and Kis A 2013 Mobility engineering and a metal–insulator transition in monolayer MoS<sub>2</sub> *Nat. Mater.* **12** 815–20
  - [7] Lembke D, Bertolazzi S and Kis A 2015 Single-layer MoS<sub>2</sub> electronics *Acc. Chem. Res.* **48** 100–10
  - [8] Azcatl A et al 2014 MoS<sub>2</sub> functionalization for ultra-thin atomic layer deposited dielectrics *Appl. Phys. Lett.* **104** 111601
  - [9] Yang J, Kim S, Choi W, Park S H, Jung Y, Cho M H and Kim H 2013 Improved growth behavior of atomic-layer-deposited high-*k* dielectrics on multilayer MoS<sub>2</sub> by oxygen plasma pretreatment *ACS Appl. Mater. Interfaces* **5** 4739–44
  - [10] Cheng L, Qin X, Lucero A T, Azcatl A, Huang J, Wallace R M, Cho K and Kim J 2014 Atomic layer deposition of a high-*k* dielectric on MoS<sub>2</sub> using trimethylaluminum and ozone *ACS Appl. Mater. Interfaces* **6** 11834–8
  - [11] Jeon T S, White J M and Kwong D L 2001 Thermal stability of ultrathin ZrO<sub>2</sub> films prepared by chemical vapor deposition on Si (100) *Appl. Phys. Lett.* **78** 368–70
  - [12] Robertson J 2006 High dielectric constant gate oxides for metal oxide Si transistors *Rep. Prog. Phys.* **69** 327–96
  - [13] Manchanda L et al 1998 Gate quality doped high K films for CMOS beyond 100 nm: 3–10 nm Al<sub>2</sub>O<sub>3</sub> with low leakage and low interface states *Technical Digest., Int. Electron Devices Meeting, 1998 IEDM'98* (Piscataway, NJ: IEEE) pp 605–8
  - [14] Balog M, Schieber M, Michman M and Patai S 1979 The characteristics of growth of films of zirconium and hafnium oxides (ZrO<sub>2</sub>, HfO<sub>2</sub>) by thermal decomposition of zirconium and hafnium β-diketonate complexes in the presence and absence of oxygen *J. Electrochem. Soc.* **126** 1203–7
  - [15] Wilk G D and Wallace R M 1999 Electrical properties of hafnium silicate gate dielectrics deposited directly on silicon *Appl. Phys. Lett.* **74** 2854–6
  - [16] Adamopoulos G, Thomas S, Wöbkenberg P H, Bradley D D, McLachlan M A and Anthopoulos T D 2011 High-mobility low-voltage ZnO and Li-doped ZnO transistors based on ZrO<sub>2</sub> high-*k* dielectric grown by spray pyrolysis in ambient air *Adv. Mater.* **23** 1894–8
  - [17] Tao J, Chai J W, Zhang Z, Pan J S and Wang S J 2014 The energy-band alignment at molybdenum disulfide and high-*k* dielectrics interfaces *Appl. Phys. Lett.* **104** 232110
  - [18] Amani M, Chin M L, Birdwell A G, O'Regan T P, Najmaei S, Liu Z, Ajayan P M, Lou J and Dubey M 2013 Electrical performance of monolayer MoS<sub>2</sub> field-effect transistors prepared by chemical vapor deposition *Appl. Phys. Lett.* **102** 193107
  - [19] Sanne A, Ghosh R, Rai A, Movva H C P, Sharma A, Rao R, Mathew L and Banerjee S K 2015 Top-gated chemical vapor deposited MoS<sub>2</sub> field-effect transistors on Si<sub>3</sub>N<sub>4</sub> substrates *Appl. Phys. Lett.* **106** 062101
  - [20] Desai S B et al 2016 MoS<sub>2</sub> transistors with 1 nm gate lengths *Science* **354** 99–102
  - [21] Zhang H, Chiappe D, Meersschaet J, Conard T, Franquet A, Nuytten T, Mannarino M, Radu I, Vandervorst W and Delabie A 2017 Nucleation and growth mechanisms of Al<sub>2</sub>O<sub>3</sub> atomic layer deposition on synthetic polycrystalline MoS<sub>2</sub> *J. Chem. Phys.* **146** 052810
  - [22] Obratsov A N 2009 Chemical vapour deposition: making graphene on a large scale *Nat. Nanotechnol.* **4** 212–3
  - [23] Wang Y, Zheng Y, Xu X, Dubuisson E, Bao Q, Lu J and Loh K P 2011 Electrochemical delamination of CVD-grown graphene film: toward the recyclable use of copper catalyst *ACS Nano* **5** 9927–33
  - [24] Zhan Y, Liu Z, Najmaei S, Ajayan P M and Lou J 2012 Large-area vapor-phase growth and characterization of MoS<sub>2</sub> atomic layers on a SiO<sub>2</sub> substrate *Small* **8** 966–71
  - [25] Yongji G et al 2017 Direct growth of MoS<sub>2</sub> single crystals on polyimide substrates *2d. Mater.* **4** 021028
  - [26] Lee C, Yan H, Brus L E, Heinz T F, Hone J and Ryu S 2010 Anomalous lattice vibrations of single- and few-layer MoS<sub>2</sub> *ACS Nano* **4** 2695–700
  - [27] McDonnell S, Brennan B, Azcatl A, Lu N, Dong H, Buie C, Kim J, Hinkle C L, Kim M J and Wallace R M 2013 HfO<sub>2</sub> on MoS<sub>2</sub> by atomic layer deposition: adsorption mechanisms and thickness scalability *ACS Nano* **7** 10354–61
  - [28] Yang W, Sun Q Q, Geng Y, Chen L, Zhou P, Ding S J and Zhang D W 2015 The integration of sub-10 nm gate oxide on MoS<sub>2</sub> with ultra low leakage and enhanced mobility *Sci. Rep.* **5** 1–9
  - [29] Buckley J, De Salvo B, Deleruyelle D, Gely M, Nicotra G, Lombardo S, Damlencourt J F, Hollinger P, Martin F and Deleonibus S 2005 Reduction of fixed charges in atomic layer deposited Al<sub>2</sub>O<sub>3</sub> dielectrics *Microelectron. Eng.* **80** 210–3
  - [30] Liu H, Si M, Deng Y, Neal A T, Du Y, Najmaei S, Ajayan P M, Lou J and Ye P D 2013 Switching mechanism in single-layer molybdenum disulfide transistors: an insight into current flow across Schottky barriers *ACS Nano* **8** 1031–8
  - [31] Liu H and Peide D Y 2012 MoS<sub>2</sub> dual-gate MOSFET with atomic-layer-deposited Al<sub>2</sub>O<sub>3</sub> as top-gate dielectric *IEEE Electron Device Lett.* **33** 546–8
  - [32] Wang H et al 2012 Large-scale 2D electronics based on single-layer MoS<sub>2</sub> grown by chemical vapor deposition *Electron Devices Meeting (IEDM) 2012* pp 4–6
  - [33] Sanne A et al 2015 Radio frequency transistors and circuits based on CVD MoS<sub>2</sub> *Nano Lett.* **15** 5039–45
  - [34] Yu L et al 2015 Enhancement-mode single-layer CVD MoS<sub>2</sub> FET technology for digital electronics *Electron Devices Meeting (IEDM) 2015* pp 32–3
  - [35] Zou X et al 2014 Interface engineering for high-performance top-gated MoS<sub>2</sub> field-effect transistors *Adv. Mater.* **26** 6255–61
  - [36] Liu J W, Liao M Y, Imura M and Koide Y 2016 High-*k* ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> bilayer on hydrogenated diamond: band configuration, breakdown field, and electrical properties of field-effect transistors *J. Appl. Phys.* **120** 124504
  - [37] Schroder K 2006 *Semiconductor Material and Device Characterization* (Hoboken: Wiley) p 345