Semiconductor Science and Technology

PAPER

Monolithic integration of GaN LEDs with vertical driving MOSFETs by selective area growth and band engineering of the p-AlGaN electron blocking layer though TCAD simulation

Recent citations

- A review on GaN-based two-terminal devices grown on Si substrates
Yu Zhang *et al*
- Improved Color Purity of Monolithic Full Color Micro-LEDs Using Distributed Bragg Reflector and Blue Light Absorption Material
Shao-Yu Chu *et al*

To cite this article: Xing Lu *et al* 2019 *Semicond. Sci. Technol.* **34** 064002

View the article online for updates and enhancements.

This content was downloaded from IP address 183.62.57.193 on 26/03/2021 at 02:49

IOP Publishing Semiconductor Science and Technology
Semicond. Sci. Technol. **34** (2019) 064002 (8pp) https://doi.org/10.1088/1361-6641/ab13e1

Monolithic integration of GaN LEDs with vertical driving MOSFETs by selective area growth and band engineering of the p-AlGaN electron blocking layer though TCAD simulation

Xing Lu[1,3], Song Yang[2], Huaxing Jiang[2] and Jin Wu[1,3]

[1] State Key Laboratory of Optoelectronic Materials and Technologies, School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou 510275, People's Republic of China
[2] Department of Electronic and Computer Engineering, the Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

E-mail: lux86@mail.sysu.edu.cn and Wujin8@mail.sysu.edu.cn

Received 25 December 2018, revised 11 March 2019
Accepted for publication 27 March 2019
Published 8 May 2019

Abstract

Based on an InGaN/GaN light emitting diode (LED) structure, monolithically integrated vertical driving metal-oxide-semiconductor field-effect transistors (MOSFETs) were designed and experimentally implemented using a selective area growth (SAG) method. A simple p-GaN/n-GaN stack was selectively regrown on top of the LED wafer to realize an n/p/n structure for the vertical MOSFET fabrication. The integrated vertical MOSFET, which can effectively modulate the injection current through the serially connected LED, exhibited high performance such as an enhancement-mode (E-mode) operation with a relatively high output current density. However, on-resistance (R_{ON}) degradation was observed in the fabricated vertical MOSFET at a low drain bias level ($V_{DS} < 2$ V). Through a 2D TCAD simulation, the origin of the high R_{ON} was revealed to be an electron barrier induced by the LED's p-AlGaN electron blocking layer (EBL). The simulation results also demonstrated that it can be improved by band engineering of the EBL.

Keywords: GaN, light emitting diode, metal-oxide-semiconductor field-effect transistor, monolithic integration, band engineering

(Some figures may appear in colour only in the online journal)

1. Introduction

GaN-based light emitting diodes (LEDs) have been extensively developed and utilized for solid-state lighting and displays by virtue of their high luminous efficacy, extremely long lifetime, and eco-friendly property compared to the traditional incandescent bulbs and fluorescent lamps [1–3]. However, dedicated electronic driving circuits, such as AC-DC power conversion, current source, and dimming control using pulse-width modulation (PWM) methods, are essential to a complete LED module. Typically, the commercially available LED drivers are implemented with discrete components and externally connected with LEDs using bonding-wires. The induced large parasitic elements can lead to a high-power consumption, low operation speed, and poor reliability of the LED modules, which has become one of the main challenges for the application of GaN-based LEDs in visible light communication (VLC), micro-displays, wearable devices, and other advanced smart-lighting systems [4–6]. To circumvent these issues, integrating LEDs with on-chip driving electronics shows a great promise and has received remarkable research interest in recent years [7].

[3] Authors to whom any correspondence should be addressed.

 © 2019 IOP Publishing Ltd Printed in the UK

On the other hand, the outstanding material properties of GaN such as a wide bandgap, large breakdown field, high electron mobility, and good thermal conductivity have spurred extensive research efforts in developing GaN-based electronic devices for power switching and RF applications [8, 9]. Currently, both lateral and vertical GaN transistors with high performance have been demonstrated [10–14]. The superior characteristics make GaN transistors excellent candidates for high-efficiency LED drivers [15]. In addition, GaN transistors and LEDs share a common material platform and can be monolithically integrated on a single chip to realize a compact smart-lighting system. Such integration scheme brings in many advantages including improved efficiency, enhanced reliability, reduced form factor and parasitics, and lower overall cost.

Previously, there have been reports on the monolithic integration of GaN LEDs with lateral-type depletion-mode (D-mode) driving transistors such as AlGaN/GaN high electron mobility transistors (HEMTs) [16–18] and lateral metal-oxide-semiconductor field-effect transistors (MOSFETs) [19]. However, D-mode operation is not preferred in the driving circuits when considering the system complexity, power consumption, and reliability issues. Integrating GaN vertical MOSFETs on an LED chip could be an alternative approach [20, 21]. Firstly, the GaN vertical MOSFETs are E-mode devices. Secondly, the vertical MOSFETs and LEDs share similar junction based vertical structures and are more suitable for integration when compared with the lateral ones.

Previously, we successfully demonstrated the concept of monolithically integrating GaN vertical driving MOSFET on LED using a selective area growth (SAG) technique [21]. In this paper, we firstly present the design considerations for such integration. An n/p/n structure for the vertical MOSFET was formed by selectively regrowing a p-GaN/n-GaN stack on top of an InGaN/GaN LED wafer. The thickness of the regrown p-GaN layer was optimized by using a 2D TCAD simulation prior fabrication, in order to prevent 'punch-through' of the n/p/n structure in the vertical MOSFET. The fabricated vertical MOSFET exhibited good performance except for a high on-resistance (R_{ON}) at a low drain bias level ($V_{DS} < 2$ V). The mechanisms underlying the R_{ON} degradation phenomenon was then systemically analyzed by simulation. In order to mitigate the R_{ON} degradation in the integrated vertical MOSFETs, a double-side graded (DG) Al composition in LED's p-AlGaN electron blocking layer (EBL) was proposed.

2. Device structure design

Figure 1 schematically shows the structural design of the monolithically integrated vertical driving MOSFET on LED. Region-① is a typical InGaN/GaN LED, which consists of, from bottom to top, an n-type GaN layer, $In_{0.16}Ga_{0.84}N$/GaN multiple quantum wells (MQWs), a p-type $Al_{0.15}Ga_{0.85}N$ EBL, and a p-type GaN layer. Region-② shows the designed vertical MOSFET connected in series with the LED via the bottom n-GaN layer. The electrode in between, namely

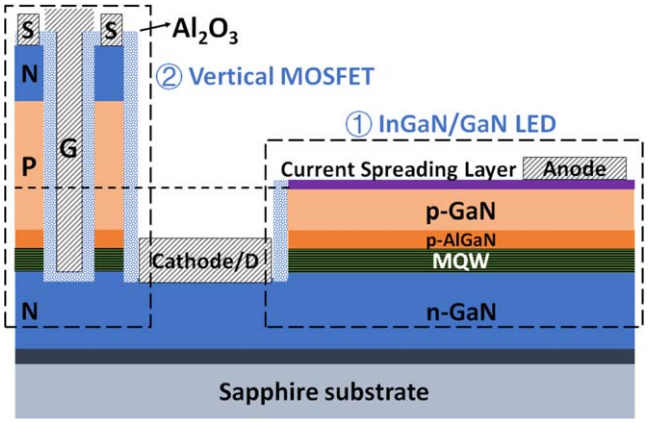

Figure 1. Schematic cross section of the monolithically integrated vertical driving MOSFET on LED.

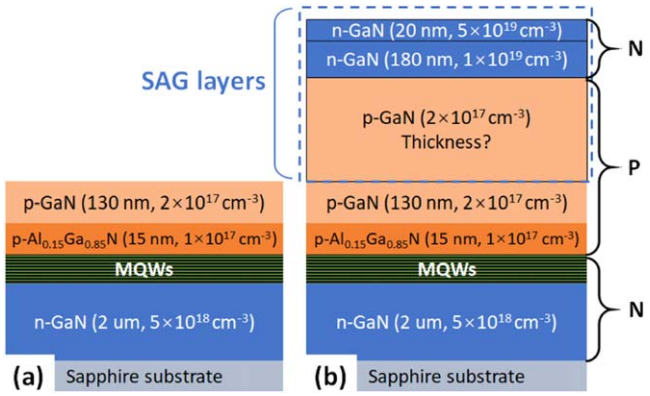

Figure 2. The (a) LED epi structure and (b) n/p/n structure for the integrated vertical MOSFET.

cathode/D, is shared by the LED and vertical MOSFET, serving as the cathode and drain electrodes, respectively. The detailed epilayer parameters of the (a) LED and (b) designed vertical MOSFET are shown in figure 2.

In order to form an n/p/n structure for the vertical MOSFET, a p-GaN/n-GaN stack rather than an n-GaN single layer was designed to be grown on the LED epi structure, since the original 130 nm-thick p-GaN layer in a LED is not thick enough and can be easily depleted in the formed n/p/n structure due to the heavily doped n-GaN layer on its both sides. Simulation in the Silvaco ATLAS was carried out to give guidance on the thickness of the regrown p-GaN layer. Source/n/p/n/drain structures with different regrown p-GaN thicknesses, as shown in figure 3(a), were constructed in the simulation to check their voltage blocking capability.

The 2D drift-diffusion model, Fermi statistics, and Shockley–Read–Hall carrier recombination model were applied in the simulation. The parallel electric field dependent mobility model with an electron saturation velocity of 1.4×10^{17} cm s^{-1} and a low-field electron mobility of n-GaN drift layer of 300 cm^2 V^{-1} · s^{-1} was also included. Source and drain are both Ohmic contacts. As the MQWs are relatively thin and have little influence on the current conduction through the n/p/n structure, they are not considered in the simulation for simplicity. The thicknesses of the total p-GaN

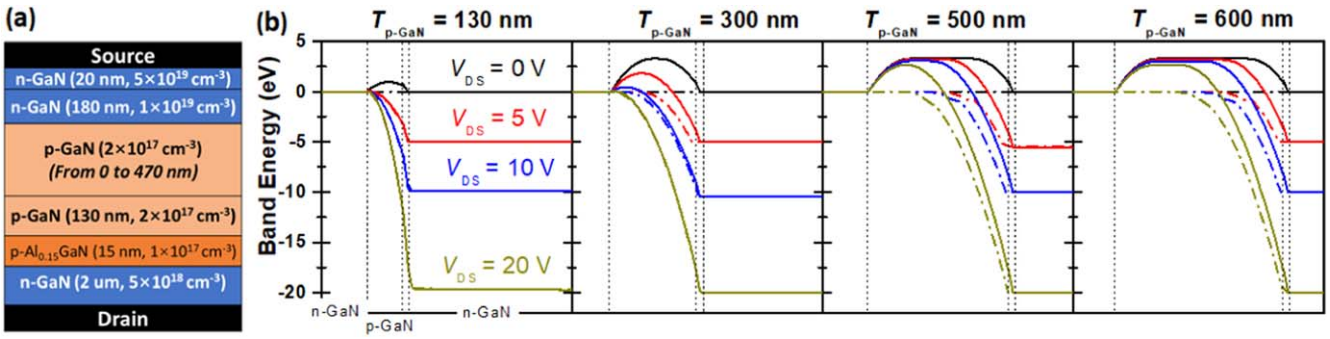

Figure 3. (a) Vertical n/p/n structure constructed in the Silvaco ATLAS for p-GaN thickness optimization. (b) Simulated conduction band diagrams for the n/p/n structures with different p-GaN thicknesses and at various V_{DS}. (The dash-dotted line represents Fermi level.)

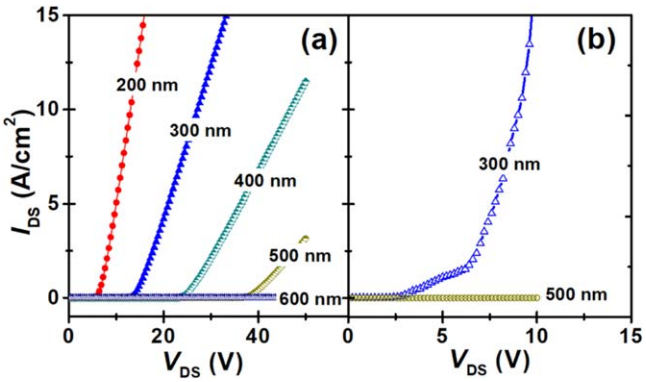

Figure 4. The (a) simulated and (b) experimental I-V curves of the n/p/n structures with different $T_{p\text{-}GaN}$.

layers ($T_{p\text{-}GaN}$) were set to 130, 200, 300, 400, 500, and 600 nm, corresponding to the regrown p-GaN thicknesses of 0, 70, 170, 270, 370, and 470 nm, respectively.

The simulated conduction band diagrams across the n/p/n structures with different $T_{p\text{-}GaN}$ and at various drain bias (V_{DS}) are plotted in figure 3(b). 'Punch-through' phenomenon happens when the p-type region within the n/p/n structure is fully depleted. As shown in figure 3(b), the 130-nm p-GaN becomes almost 'punch-through' even at $V_{DS} = 0$ V, which is depleted by the build-in electric field of the two pn junctions, proving the necessity of thickening the p-GaN layer. On the other hand, a very thick p-GaN layer in the n/p/n structure will bring in high channel resistance, restricting the driving capability of the vertical MOSFET. Considering that the turn-on voltage of a typical LED is relatively low (~3 V), a V_{DS} up to 10 V can satisfy most of the operation conditions for an LED driver. According to the simulated I-V curves in figure 4(a), two n/p/n structures were fabricated by regrowing p-GaN/n-GaN stacks on LED wafers to simulate the integration process, with $T_{p\text{-}GaN}$ of 300 nm and 500 nm. Figure 4(b) shows the measured I-V curves of the fabricated n/p/n structures. The deviation of the voltage blocking capabilities between the simulated and experimental results might be due to the yet-to-be-perfect GaN crystalline quality and the influence of the regrowth interface. Finally, a $T_{p\text{-}GaN}$ of 500 nm was chosen as an optimized design in our integration strategy, being able to provide a voltage blocking capability of over 10 V for the integrated vertical MOSFET.

3. Device fabrication and characterization

3.1. Device fabrication

The device fabrication in this work started with an InGaN/GaN LED wafer grown on a 2-inch patterned sapphire substrate. First, a 200 nm SiO_2 regrowth hard mask was deposited on the LED wafer by plasma enhanced chemical vapor deposition (PECVD) and patterned using a buffered oxide etchant (BOE), as shown in figure 5(a). Then, the selective regrowth of a p-GaN/n-GaN stack on the wafer was performed in an Aixtron 2400HT metal organic chemical vapor deposition (MOCVD) system, as shown in figure 5(b). The p-GaN activation process was conducted *in situ* in the MOCVD chamber. As designed, the thicknesses of the regrown p- and n-GaN layers were 370 nm and 200 nm, respectively. The Mg doping concentration and hole concentration in p-GaN are 3×10^{19} cm^{-3} and 2×10^{17} cm^{-3}, respectively. After removal of the regrowth mask by BOE, the gate trenches of the vertical MOSFETs and device isolation for both the LEDs and MOSFETs were etched simultaneously using a two-step dry/wet etching process combining a Cl_2-based inductively coupled plasma (ICP) etch and a TMAH solution etch (figure 5(c)), where the wet etch can help smoothing the etched GaN sidewall surface and improving the channel electron mobility of the vertical MOSFETs. A 30-nm thick Al_2O_3 film was then blanket deposited by atomic layer deposition (ALD) on the sample (figure 5(d)), serving as the both the gate dielectric of the MOSFETs and the passivation for the devices. After removing the Al_2O_3 passivation in the LED region, a thin Ni/Au (3/3 nm) metal stack was deposited by e-beam evaporation followed by a rapid thermal annealing (RTA) in an atmospheric ambient at 570 °C for 5 min, to form the LEDs' transparent current spreading layer (figure 5(e)). Finally, two steps of metallization were carried out, including the MOSFETs' source/gate/drain electrodes and LEDs' cathode/anode electrodes (figure 5(f)). The MOSFETs' gate metal was Ni. Figure 6 shows the layout and scanning electron microscopy (SEM) image of the integrated VMOSFET. The device is circular in shape, with a diameter of 30 μm. The connection between the LED and vertical driving MOSFET was realized through the highly conductive bottom n-GaN layer.

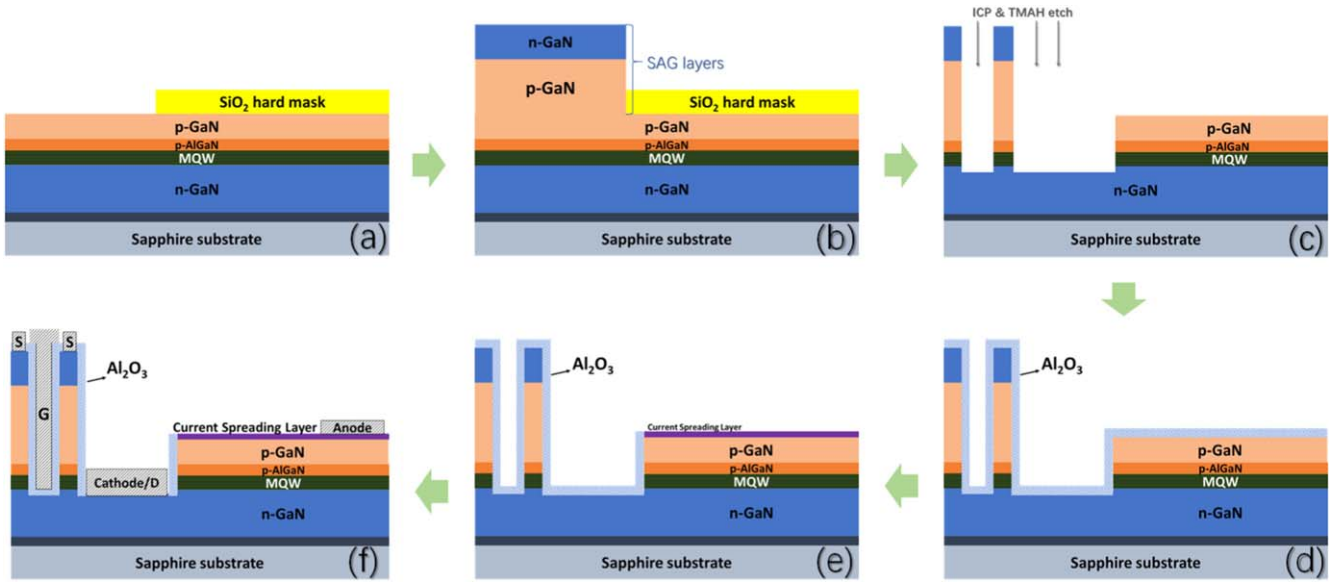

Figure 5. Schematics of the fabrication process steps for the monolithically integrated vertical driving MOSFET on LED.

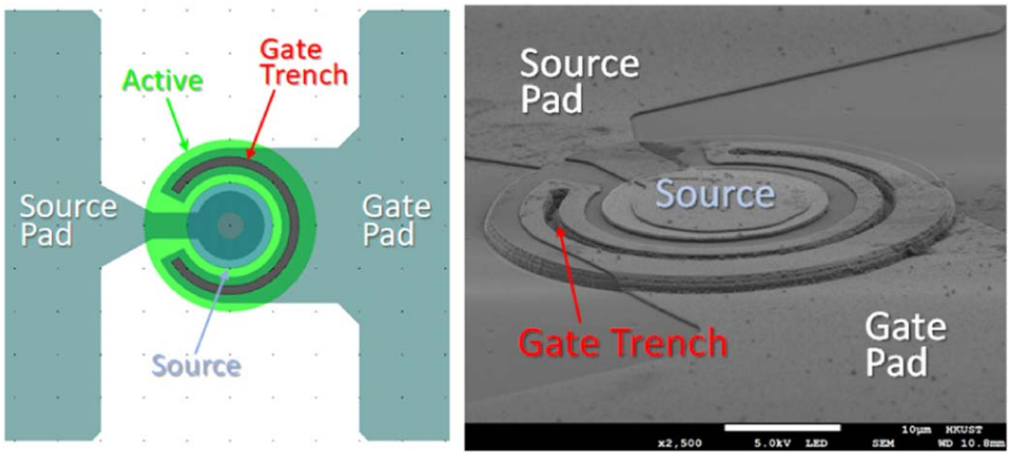

Figure 6. Layout and SEM image of the integrated vertical MOSFET on LED.

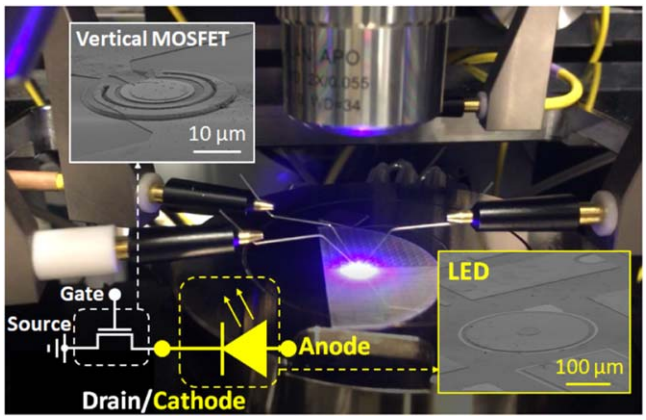

Figure 7. The on-testing integrated device emits blue light. The insets show the equivalent circuit diagram and SEM images of the fabricated devices.

3.2. Device characterization

Figure 7 shows the on-testing integrated device emitting blue light, whose brightness can be modulated by adjusting the gate bias of the vertical MOSFET. The insets show the equivalent circuit diagram and SEM images of the fabricated devices.

The measured transfer curve of the individual vertical MOSFET is plotted in figure 8(a). The vertical MOSFET is E-mode with a threshold voltage (V_{th}) of +1.8 V and the off-state current density (I_{off}) at $V_{GS} = 0$ V is as low as 4×10^{-2} A cm^{-2}. Figure 8(b) shows the measured output curves of the individual vertical MOSFET and integrated device. The maximum output current density of the vertical MOSFET exceeds 1.4 kA cm^{-2} at $V_{DS} = 8$ V and $V_{GS} = 9$ V. However, a R_{ON} degradation was observed for the fabricated device at a low drain bias level ($V_{DS} < 2$ V). The high R_{ON}, which will lead to a high-power consumption and low efficiency of the driver, has to be eliminated.

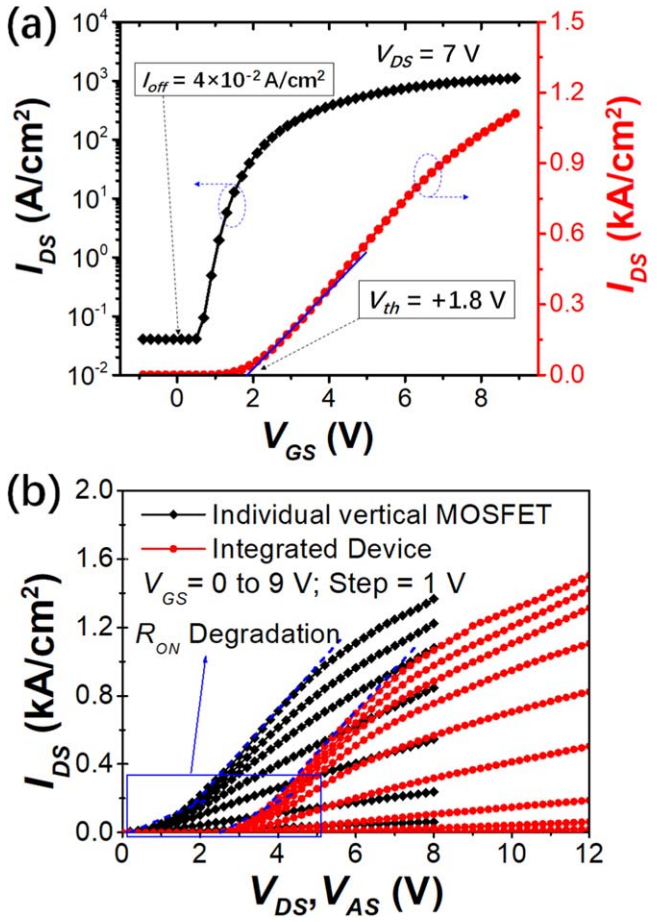

Figure 8. (a) Measured transfer (a) and output (b) curves of the fabricated devices.

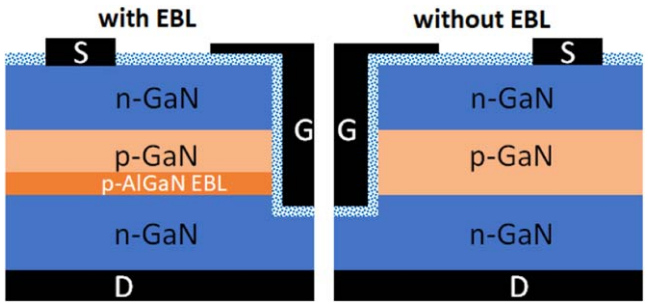

Figure 9. Schematic cross-section of the simulated half-cell vertical MOSFET with and without the p-AlGaN EBL.

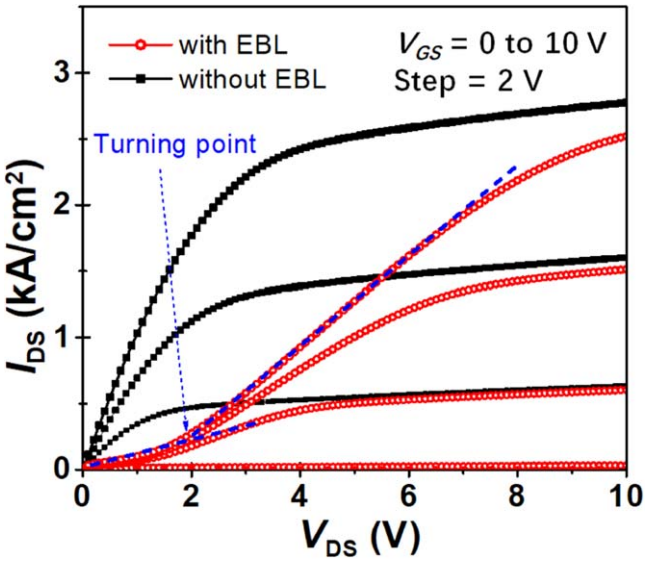

Figure 10. Simulated output curves of the vertical MOSFETs with and without the p-AlGaN EBL.

4. EBL influence and band engineering

4.1. Mechanisms of R_{ON} degradation

Firstly, the suspicion that poor Ohmic contact results in a high R_{ON} can be ruled out in this work. The source and drain Ohmic contacts in the device were formed using a Cr/Al/Ti/Au metal stack deposited on the highly doped n-GaN layers and very small contact resistance could be easily achieved even without annealing.

When comparing to the conventional GaN vertical MOSFETs in [13, 14], the integrated device in this study consists of an extra p-$Al_{0.15}Ga_{0.85}N$ EBL. In order to investigate the influence of the EBL on the performance of the integrated vertical MOSFET, devices with and without the p-$Al_{0.15}Ga_{0.85}N$ EBL (in figure 9) were simulated and compared in the Silvaco ATLAS. The bandgap energies and band offset of the $Al_xGa_{1-x}N$ ternary alloys in the simulation referred to [22] and are listed in table 1. The thickness and dopants concentration for each layer are kept the same with the experiments.

The simulated output curves of the vertical MOSFETs with and without the p-$Al_{0.15}Ga_{0.85}N$ EBL are plotted in figure 10. It can be clearly seen that the R_{ON} degradation phenomenon, similar to the experimental result, occurred on the device with the EBL, while the device without an EBL showed typical output curves. Therefore, the p-$Al_{0.15}Ga_{0.85}N$ EBL has been proved to be the culprit of the high R_{ON} in the integrated vertical MOSFET.

Table 1. The physical parameters used in the simulation.

Parameter	Value
GaN Band Gap	3.4 eV
$Al_xGa_{1-x}N$ band gap	6.13x + 3.42(1 − x) −x(1 − x) eV
Band offset	$\Delta E_C = 0.7 \times (E_g^{AlGaN} - E_g^{GaN})$
Gate metal work function	5.1 eV
Al_2O_3 dielectric constant	9.3

To help explaining the underlying mechanisms, a sketch map showing the electrons' flowing directions in both the LED and integrated vertical MOSFET is drawn in figure 11. A p-$Al_{0.15}Ga_{0.85}N$ EBL is always intentionally adopted in LEDs to form an electron barrier and block electrons from flowing out of MQWs active region, and consequently increasing the LEDs' radiative recombination rate and light output power (LOP) [23], as shown in process-① in the inset of figure 11. However, an unwanted electron barrier also existed at the p-GaN/p-$Al_{0.15}Ga_{0.85}N$ interface in the integrated vertical MOSFET, resulting in serious R_{ON} degradation

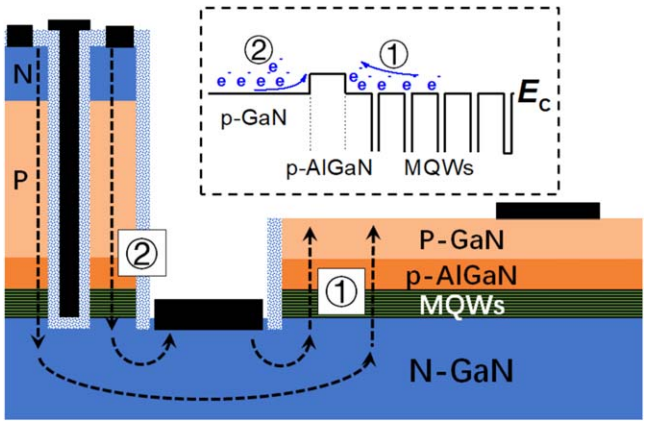

Figure 11. Sketch map shows the flowing directions of electrons in the (process-①) LED and (process-②) integrated vertical MOSFET. Inset illustrates the influence of the p-$Al_{0.15}Ga_{0.85}N$ EBL on the electrons flowing.

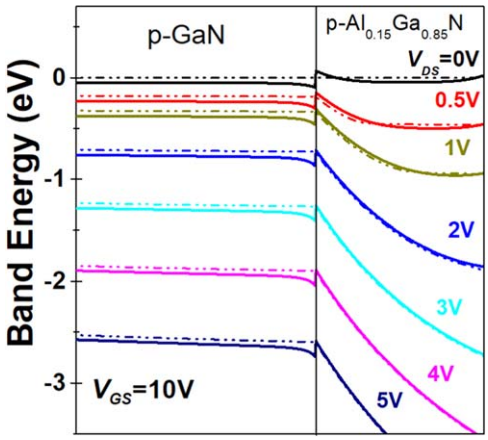

Figure 12. Simulated conduction band diagrams of the vertical MOSFET with the p-$Al_{0.15}Ga_{0.85}N$ EBL at different V_{DS}. (The dash-dotted line represents Fermi level.).

of the device, as illustrated in process-②. Figure 12 plots the simulated conduction band diagrams of the vertical MOSFET across the p-GaN/p-$Al_{0.15}Ga_{0.85}N$ interface with different V_{DS} and at $V_{GS} = 10$ V. An electron barrier located at the p-GaN/p-$Al_{0.15}Ga_{0.85}N$ interface can be clearly observed. With the increase of V_{DS}, the electron barrier height is reduced. As shown in figures 8 and 10, the turning points in the output curves of the fabricated and simulated vertical MOSFETs are both located at $V_{DS} \approx 2$ V, suggesting that an extra drain bias of ~2 V is needed to overcome the EBL-induced electron barrier in the integrated devices.

4.2. Band engineering of EBL

The R_{ON} degradation problem in the integrated vertical MSOFETs can be resolved through band engineering of the EBL, since it results from the electron barrier induced by the uniform p-$Al_{0.15}Ga_{0.85}N$ EBL currently used in the LEDs.

A novel p-$Al_xGa_{1-x}N$ EBL with a double-side graded Al composition was proposed for the integrated devices, as schematically shown in figure 13. To maintain an effective

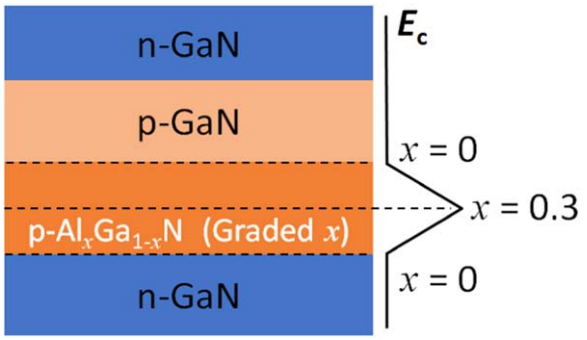

Figure 13. Proposed p-$Al_xGa_{1-x}N$ EBL with a double-side graded Al composition.

electron barrier for the LEDs, the peak Al composition was set to 0.3 [24] for the DG EBL and the thickness was increased from 15 nm to 25 nm.

A vertical MOSFET with the proposed DG p-$Al_xGa_{1-x}N$ EBL was constructed and simulated in the Silvaco ATLAS, and compared to the devices with the uniform p-$Al_{0.15}Ga_{0.85}N$ EBL and without an EBL. Figure 14 plots the simulated conduction band diagrams for the two devices with different EBLs at various V_{GS} (from 0 to 10 V) and $V_{DS} = 0$ V.

As can easily be seen, the barrier height for the device with a uniform EBL remained relatively high even when the channel was fully turned on at $V_{GS} = 10$ V, which is mainly due to the abrupt conduction band offset at the p-GaN/p-$Al_{0.15}Ga_{0.85}N$ interface. On the contrary, the barrier height in the device with a DG EBL lowered markedly with the increase of V_{GS} and became much easier for electrons to surmount. Figure 15 compares the simulated output curves for the three vertical MOSFETs with the DG EBL, with uniform EBL, and without an EBL. The R_{ON} degradation phenomenon was successfully eliminated by applying the proposed DG EBL in the device.

The performance of an LED with the proposed DG p-$Al_xGa_{1-x}N$ EBL was also investigated by simulation and compared with that using the conventional uniform p-$Al_{0.15}Ga_{0.85}N$ EBL. The structural parameters used in the simulation were consistent with those shown in figure 2(a) except for the two different EBLs. Commonly accepted physical models including the spontaneous and piezoelectric polarization models, Auger recombination model with a coefficient of 2×10^{-30} $cm^6\,s^{-1}$, and radiative recombination model with a coefficient of 10^{-11} $cm^3\,s^{-1}$ were employed in the simulation, as suggested in [24, 25]. Figure 16 compares the simulated LOP and internal quantum efficiency (IQE) characteristics between the two LEDs with different EBLs as a function of the injection current. It can be found that the proposed DG EBL, instead of degrading the LED's performance, increases its LOP and IQE at a high injection current level. Comparing to the uniform EBL, the DG EBL can reduce the hole barrier on valence band at the EBL/MQWs interface and increase the hole injection efficiency of an LED [24, 26–28]. Consequently, the LOP and IQE of the

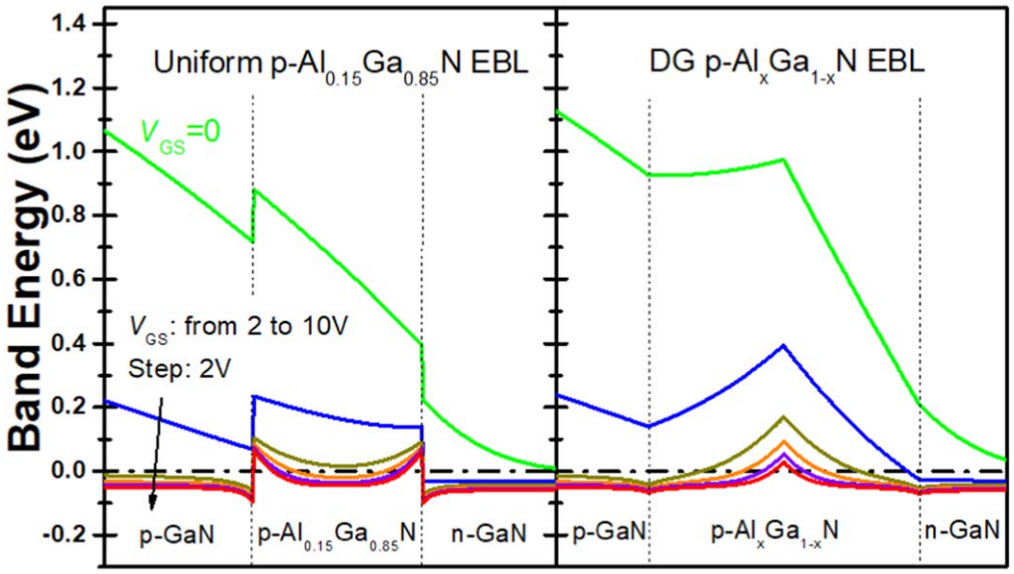

Figure 14. Simulated conduction band diagrams for the two vertical MOSFETs with different EBLs at various V_{GS} (from 0 to 10 V) and $V_{DS} = 0$ V. (The dash-dotted line represents Fermi level.)

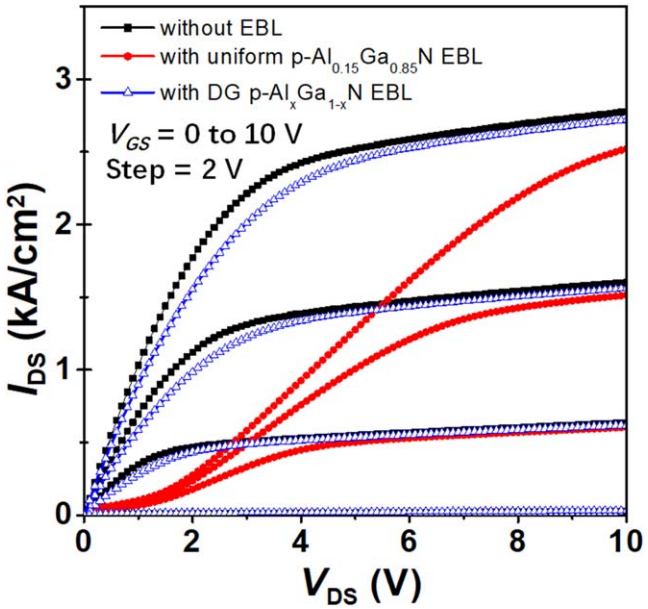

Figure 15. Simulated output curves of the vertical MOSFETs with the DG EBL, the uniform EBL, and without EBL.

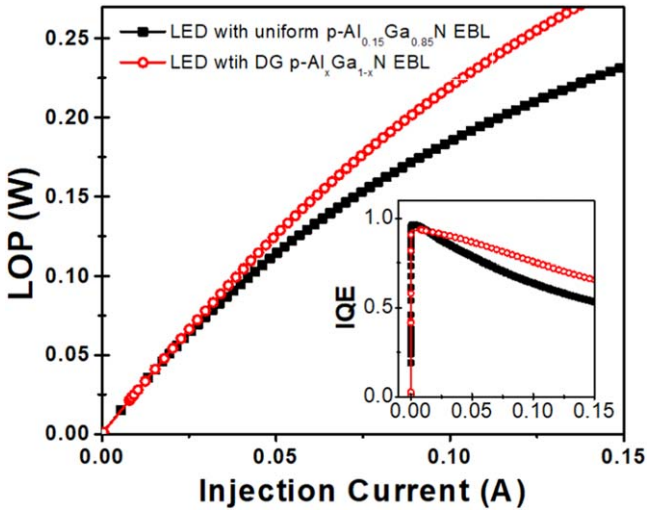

Figure 16. Simulated LOP characteristics of the two LEDs with the uniform and DG EBLs. The inset compares the two LEDs' IQE.

LED can be improved, especially at a high injection current level [24, 26].

5. Conclusion

In summary, monolithically integrated vertical driving MOSFETs were designed and fabricated based on an InGaN/GaN LED epi structure and using a SAG method. Prior to device fabrication, simulation in the Silvaco ATLAS was performed to optimize the regrown p-GaN thickness for the formation of a proper n/p/n structure for the vertical MOSFET. The fabricated E-mode vertical MOSFET exhibited a relatively high output current density of exceeding 1.4 kA cm^{-2}. However, R_{ON} degradation phenomenon was observed for the device at a low V_{DS} level (below 2 V). An electron barrier that induced by the uniform p-$Al_{0.15}Ga_{0.85}N$ EBL buried within the integrated vertical MOSFET turned out to be the culprit of the high R_{ON}. A novel DG p-$Al_xGa_{1-x}N$ EBL was proposed for the integrated devices and proven highly effective in mitigating the R_{ON} degradation by simulation. Meanwhile, a relatively high LOP and IQE could be maintained for the LEDs using the proposed DG EBL.

Acknowledgments

This work was supported in part by the International Science and Technology Cooperation Program of Guangzhou under

Grant No. 201807010093 and the Frontier and Key Technological Innovation Foundation of Guangdong Province under grant 2017A050506039.

ORCID iDs

Xing Lu https://orcid.org/0000-0001-5808-9552
Jin Wu https://orcid.org/0000-0002-3065-6858

References

[1] Pimputkar S, Speck J S, Denbaars S P and Nakamura S 2009 Prospects for LED lighting *Nature Photon* **3** 180–2
[2] Crawford M H 2009 LEDs for solid-state lighting: performance challenges and recent advances *IEEE J. Sel. Top. Quant. Electro* **15** 1028–40
[3] Shur M S and Zukauskas R 2005 Solid-state lighting: towards superior illumination *Proc. of IEEE Conf.* (IEEE) pp 1691–703
[4] McKendry J J D, Massoubre D, Zhang S, Rae B R, Green R P, Gu E, Hemderson R K, Kelly A E and Dawson M D 2012 Visible-light communications using a CMOS-controlled micro-light-emitting-diode array *J. Ligntwave Technol.* **30** 61–7
[5] Gong C-S A, Lee Y-C, Lai J-L, Yu C-H and Yang C-Y 2016 The high-efficiency LED driver for visible light communication applications *Presented at the Eighth Int. Conf. on Ubiquitous and Future Networks (ICUFN)* (Vienna, Austria) *(5–8 Jul*
[6] Karlicek R F 2012 Smart lighting-beyond simple illumination *Proc. of IEEE Conf. on Photonics Socoety Summer Topical Meeting Series* (IEEE) pp 147–8
[7] Lau K M, Choi H W, Lee S R, Mok P K T, Sin J K O, Yue C P and Ki W H 2013 Cost-effective and eco-friendly LED system-on-a-chip (SoC) *Proc. of the 10th China Int. Forum Solid State Lighting* (Acadamic) pp 235–8
[8] Mishra U K, Shen L, Kazior T E and Wu Y F 2008 GaN-based RF power devices and amplifiers *Proc. of IEEE Conf.* (IEEE) pp 287–305
[9] Kuzuhara M and Tokuda H 2015 Low-loss and high-voltage III-nitride transistors for power switching applications *IEEE T. Electron Devices* **62** 405–13
[10] Shinohara K *et al* 2013 Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications *IEEE T. Electron Devices* **60** 2982–96
[11] Jiang H, Liu C, Chen Y, Lu X, Tang C W and Lau K M 2017 Investigation of *in situ* SiN as gate dielectric and surface passivation for GaN MISHEMTs *IEEE T. Electron Devices* **64** 832–9
[12] Lu X, Ma J, Jiang H, Liu C, Xu P and Lau K M 2015 Fabrication and characterization of gate-last self-aligned AlN/GaN MISHEMTs with *in situ* SiNx gate dielectric *IEEE T. Electron Devices* **62** 1862–9
[13] Li R, Cao Y, Chen M and Chu R 2016 600 V/1.7 Ω normally-off GaN vertical trench metal–oxide–semiconductor field-effect transistor *IEEE Electron Device Lett.* **37** 1466–9
[14] Liu C, Khadar R A and Matioli E 2018 GaN-on-Si quasi-vertical power MOSFETs *IEEE Electron Device Lett.* **39** 71–4
[15] Bandyopadhyay S, Neidorff B, Freeman D and Chandrakasan A P 2013 90.6% efficient 11MHz 22W LED driver using GaN FETs and burst-mode controller with 0.96 power factor *Proc. of IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers* (IEEE) pp 368–9
[16] Li Z, Waldron J, Detchprohm T, Wetzel C, Karlicek R F and Chow T P 2013 Monolithic integration of light-emitting diodes and power metal-oxide-semiconductor channel high-electron-mobility transistors for light-emitting power integrated circuits in GaN on sapphire substrate *Appl. Phys. Lett.* **102** 192107
[17] Liu Z, Huang T, Ma J, Liu C and Lau K M 2014 Monolithic integration of AlGaN/GaN HEMT on LED by MOCVD *IEEE Electron Device Lett.* **35** 330–2
[18] Kalaitzakis F G, Iliopoulos E, Konstantinidis G and Pelekanos N T 2012 Monolithic integration of nitride-based transistor with light emitting diode for sensing applications *Microelectron. Eng.* **90** 33–6
[19] Lee Y J *et al* 2014 Monolithic integration of GaN-based light-emitting diodes and metal-oxide-semiconductor field-effect transistors *Opt. Express* **22** 1589–A1595
[20] Lu X, Liu C, Jiang H, Zou X, Zhang A and Lau K M 2016 Monolithic integration of enhancement-mode vertical driving transistors on a standard InGaN/GaN light emitting diode structure' *Appl. Phys. Lett.* **109** 053504
[21] Lu X, Liu C, Jiang H, Zou X and Lau K M 2017 High performance monolithic integrated GaN driving VMOSFET on LED *IEEE Electronic Device Lett.* **38** 752–5
[22] Ambacher O, Smart J, Shealy J R, Weimann N G, Chu K, Murphy M, Schaff W J and Eastman L F 1999 Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures *J. Appl. Phys.* **85** 3222–33
[23] Han S, Lee D, Lee S, Cho C, Kwon M, Lee S P, Noh D Y, Kim D, Kim Y C and Park S 2009 Effect of electron blocking layer on efficiency droop in InGaN/GaN multiple quantum well light-emitting diodes *Appl. Phys. Lett.* **94** 231123
[24] Wang C *et al* 2010 Hole injection and efficiency droop improvement in InGaN/GaN light-emitting diodes by band-engineered electron blocking layer *Appl. Phys. Lett.* **197** 261103
[25] Park J H, Kim D Y, Hwang S, Meyaard D, Schubert E F, Han Y D, Choi J W, Cho J and Kim J K 2013 Enhanced overall efficiency of GaInN-based light-emitting diodes with reduced efficiency droop by Al-composition-graded AlGaN/GaN superlattice electron blocking layer *Appl. Phys. Lett.* **103** 061104
[26] Kuo Y, Chang J and Tsai M 2010 Enhancement in hole-injection efficiency of blue InGaN light-emitting diodes from reduced polarization by some specific designs for electron blocking layer *Opt. Lett.* **35** 3285–7
[27] Sun P, Dang S, Li T, Li C, Zhang H, Sun C and Xu B 2014 Carrier transport improvement in blue InGaN light-emitting diodes via reduced polarization using a band-engineering electron blocking layer *J. Disp. Technol.* **10** 1102–5
[28] Zhang N, Liu Z, Wei T, Zhang L, Wei X, Wang X, Lu H, Li J and Wang J 2012 Effect of the graded electron blocking layer on the emission properties of GaN-based green light-emitting diodes *Appl. Phys. Lett.* **100** 053504