

# Off-state drain leakage reduction by post metallization annealing for Al<sub>2</sub>O<sub>3</sub>/GaN/AlGa<sub>0.3</sub>N/GaN MOSHEMTs on Si

Huaxing Jiang<sup>1</sup>, Xing Lu<sup>2</sup>, Chao Liu<sup>1</sup>, Qiang Li<sup>1</sup>, and Kei May Lau<sup>\*1</sup>

<sup>1</sup> Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

<sup>2</sup> State Key Laboratory of Electrical Insulation and Power Equipment, School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, P. R. China

Received 15 September 2015, revised 13 November 2015, accepted 2 December 2015

Published online 23 December 2015

**Keywords** annealing, drain leakage, GaN, high electron mobility transistors, metallization, metal–oxide–semiconductor structures

\* Corresponding author: e-mail eekmlau@ust.hk, Phone: +852 2358 7049, Fax: +852 2358 1485

Impact of post metallization annealing (PMA) on the off-state drain leakage ( $I_{\text{off}}$ ) for Al<sub>2</sub>O<sub>3</sub>/GaN/AlGa<sub>0.3</sub>N/GaN metal-oxide-semiconductor high electron mobility transistors (MOSHEMTs) on Si has been investigated. After implementation of PMA at 500 °C for 10 min in N<sub>2</sub> ambient, the  $I_{\text{off}}$  can be reduced by three orders of magnitude compared to that without PMA. In consequence, a high on/off current ratio of 10<sup>8</sup> and a steep subthreshold slope of 71 mV/dec are achieved for the MOSHEMTs. The reduction of  $I_{\text{off}}$  results from the suppression of source-drain surface leakage through the interface between Al<sub>2</sub>O<sub>3</sub> and GaN. The decrease of

accumulation capacitance of the MOS capacitors (MOSCAPs) after 500 °C PMA suggests an oxidation process at the GaN surface during the high temperature annealing, which was confirmed by the increase of oxide layer thickness measured by transmission electron microscopy (TEM), and also the increase of Ga–O/Ga–N bond ratio at the Al<sub>2</sub>O<sub>3</sub>/GaN interface revealed by X-ray photoelectron spectroscopy (XPS). These results suggest that the significant reduction of  $I_{\text{off}}$  after 500 °C PMA can be attributed to partial surface oxidation of the GaN cap, which suppresses the conduction path at the Al<sub>2</sub>O<sub>3</sub>/GaN interface.

© 2015 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

**1 Introduction** GaN-based high electron mobility transistors (HEMTs) have demonstrated great potential for power switching and high frequency power amplifier applications [1–3]. The conventional HEMT with Schottky gate structure usually suffers from high gate leakage, which would increase the standby power loss and also limit the gate forward bias. In order to block the gate leakage current and suppress the drain current collapse, the Al<sub>2</sub>O<sub>3</sub> gate dielectric by atomic layer deposition (ALD) has been adopted to form metal-oxide-semiconductor HEMTs (MOSHEMTs) [4–7]. However, adding an insulator between the gate metal and barrier layer creates an extra dielectric/(Al)GaN interface, which could introduce high density donor-like interface traps [8, 9]. These trap states can assist the two-dimensional variable range hopping (2D-VRH) conduction, resulting in serious surface leakage

current through the interface [10, 11]. Consequently, a high off-state drain leakage current ( $I_{\text{off}}$ ) can be a serious issue for the MOSHEMTs. Post metallization annealing (PMA) has been studied to improve the gate contact with dielectric and also to reduce the fixed charges at the dielectric/semiconductor interface or within the dielectric bulk [12–16]. Most of these studies mainly focus on the influence of PMA on the threshold voltage of MOSHEMTs.

In this work, we investigated the effects of PMA on the  $I_{\text{off}}$  for Al<sub>2</sub>O<sub>3</sub>/GaN/AlGa<sub>0.3</sub>N/GaN MOSHEMTs on Si. It was found that PMA at 500 °C in N<sub>2</sub> for 10 min can reduce the  $I_{\text{off}}$  by three orders of magnitude, resulting in a high on/off current ratio of 10<sup>8</sup> and a steep subthreshold slope (SS) of 71 mV/dec. The reduction of accumulation capacitance of the MOS capacitors (MOSCAPs) after 500 °C PMA revealed a partial oxidation of the GaN surface.

Transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) techniques were performed to identify the oxidation process at the  $\text{Al}_2\text{O}_3/\text{GaN}$  interface during the high temperature annealing.

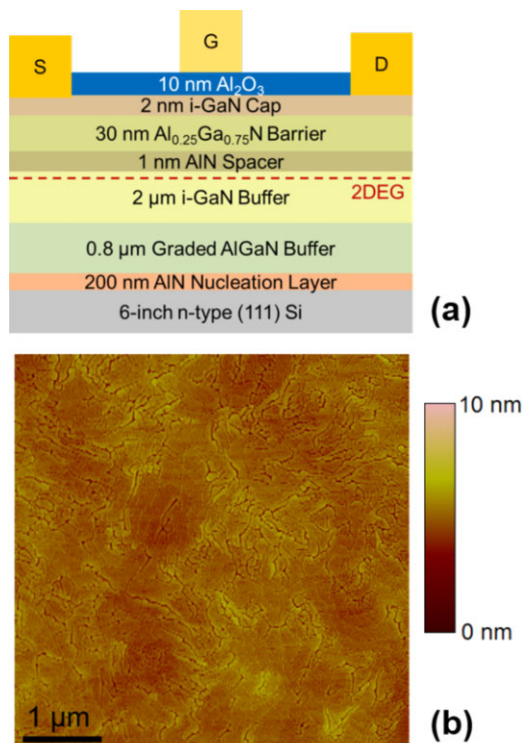
**2 Experimental** The GaN/AlGaIn/GaN heterostructure used in this work was grown on a 6-inch n-type Si substrate by metal-organic chemical vapor deposition (MOCVD). As shown in Fig. 1(a), the epilayer, from bottom to top, consists of a 200-nm AlN nucleation layer, an 800-nm step-graded AlGaIn layer, a 2- $\mu\text{m}$  unintentionally doped GaN layer, a 1-nm AlN spacer, a 30-nm  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$  barrier, and a 2-nm GaN cap. Hall measurements showed a sheet carrier density of  $7 \times 10^{12} \text{ cm}^{-2}$  and mobility of  $1800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , resulting in an average sheet resistance of  $500 \Omega/\text{sq}$ . Atomic force microscope (AFM) observation of the as-grown HEMT epi on Si showed a smooth surface morphology with root mean square (RMS) roughness of 0.5 nm across a  $5 \times 5 \mu\text{m}^2$  scanned area.

The MOSHEMT fabrication started from device isolation by  $\text{BCl}_3/\text{Cl}_2$ -based inductively coupled plasma (ICP) etching. The mesa depth was around 150 nm. Then the source/drain metal stack Ti/Al/Ni/Au (20/150/50/80 nm) was deposited by e-beam evaporation and annealed at  $850^\circ\text{C}$  in  $\text{N}_2$  ambient for 30 s to form Ohmic contact. After that, the sample was cleaned by an oxygen plasma treatment with a power of 100 W for 1 min and a  $\text{HCl}:\text{H}_2\text{O}$  (1:3) solution immersion for 2 min. Then a 10-nm  $\text{Al}_2\text{O}_3$  gate

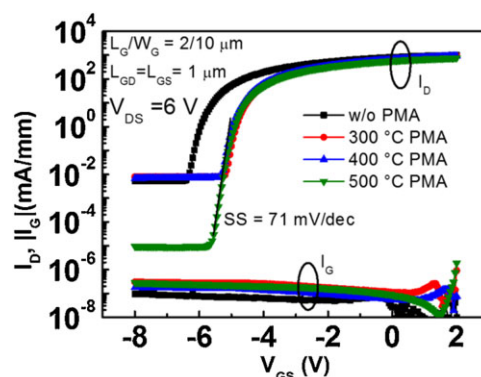
dielectric was deposited immediately in an Oxford Instruments atomic layer deposition (ALD) system at  $300^\circ\text{C}$  using trimethylaluminum (TMA) and  $\text{H}_2\text{O}$  vapor as precursors. Finally the Ni/Au (20/200 nm) gate metal was deposited by e-beam evaporation. After device fabrication, the sample was separated into four pieces, three of which were annealed at 300, 400, and  $500^\circ\text{C}$ , respectively, by rapid thermal annealing (RTA) process in  $\text{N}_2$  ambient for 10 min. The MOSHEMTs used in the following characterization are with 2  $\mu\text{m}$  gate length, gate-source and gate-drain distance of 1  $\mu\text{m}$ , and gate width of 10  $\mu\text{m}$ . Circular MOSCAPs with 200  $\mu\text{m}$  in diameter were also fabricated on the same sample for capacitance–voltage (CV) characterization.

**3 Results and discussion** Figure 2 shows the drain current and gate leakage current versus gate bias for the fabricated MOSHEMTs. For all the devices without and with various PMAs, the gate leakage currents remain below  $10^{-6} \text{ mA mm}^{-1}$ . The devices without PMA show a high  $I_{\text{off}}$  of  $10^{-2} \text{ mA mm}^{-1}$  at  $V_{\text{GS}}$  of  $-8 \text{ V}$  and  $V_{\text{DS}}$  of 6 V. The large difference between the gate leakage current and the  $I_{\text{off}}$  indicates that the  $I_{\text{off}}$  is dominated by the drain-to-source leakage. No obvious change in the  $I_{\text{off}}$  is observed for the devices with PMA at  $300^\circ\text{C}$  and  $400^\circ\text{C}$ , while the  $I_{\text{off}}$  is reduced by three orders of magnitude for the devices with PMA at  $500^\circ\text{C}$ . Consequently, a high  $I_{\text{on}}/I_{\text{off}}$  ratio of  $\sim 10^8$  and a sharp SS of 71 mV/dec are achieved for the MOSHEMTs with  $500^\circ\text{C}$  PMA. The positive shift of threshold voltage for samples with PMA was attributed to the reduction of fixed positive charges at the  $\text{Al}_2\text{O}_3/\text{GaN}$  interface or within  $\text{Al}_2\text{O}_3$  bulk [12, 13].

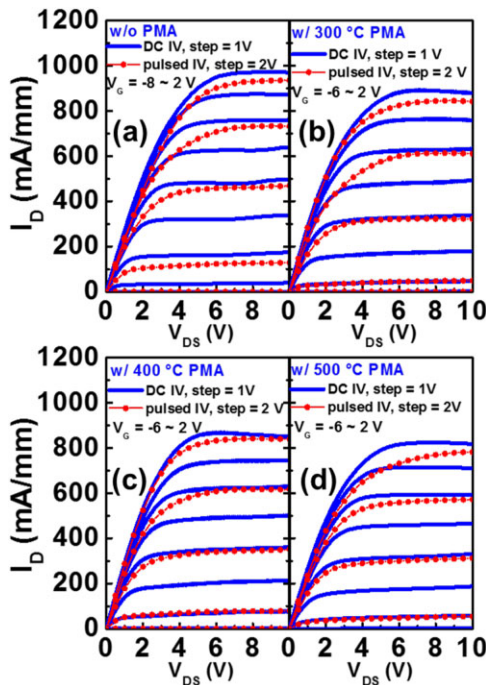
In order to find out the impact of PMA on the effectiveness of the  $\text{Al}_2\text{O}_3$  passivation in the access region, DC-pulsed IV dispersion of output characteristics for the MOSHEMTs without PMA and with various PMA conditions were characterized, as compared in Fig. 3. For the DC output characteristics, the maximum drain current at the gate bias of +2 V for the device with  $500^\circ\text{C}$  PMA is  $\sim 20\%$  lower than that without PMA. This is partially due to the positive shift of the threshold voltage after  $500^\circ\text{C}$  PMA, which reduces the gate overdrive voltage. On the other hand,



**Figure 1** (a) Cross-sectional schematic of fabricated MOSHEMTs and (b) AFM image with  $5 \times 5 \mu\text{m}^2$  scan for the as-grown GaN/AlGaIn/GaN HEMT structure on Si.



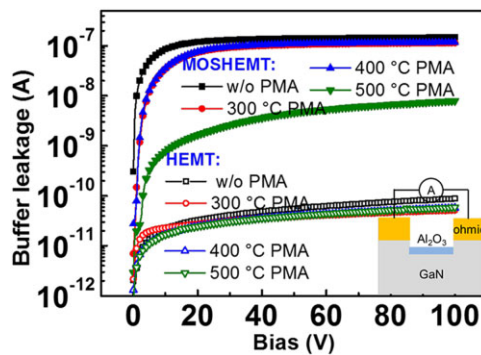
**Figure 2** Comparison of drain and gate current versus gate bias of devices without and with different PMAs at  $V_{\text{DS}}$  of 6 V.



**Figure 3** DC/gate pulsed output characteristics of the MOSHEMTs (a) without PMA, (b) with 300 °C PMA, (c) with 400 °C PMA, and (d) with 500 °C PMA. The pulse period is 1 s and pulse width is 500  $\mu$ s. Gate pulse base voltage  $V_{GS0}$  is  $-8$  V.

the sheet resistance ( $R_{sh}$ ) and Ohmic contact resistance ( $R_c$ ), measured 387  $\Omega$ /sq and 1.1  $\Omega \cdot \text{mm}$  without PMA, slightly increase to 400  $\Omega$ /sq and 1.2  $\Omega \cdot \text{mm}$  after 500 °C PMA. The slight increase of  $R_{sh}$  and  $R_c$  may have contributed to the decrease of maximum drain current. For the pulsed IV characterization, a pulsed voltage with duty/period of 500  $\mu$ s/1 s was applied to the gate with the base voltage at  $-8$  V (quiescent bias at pinch-off condition). On-state resistance ( $R_{on}$ ) was extracted in the linear region with gate bias of  $+2$  V and compared between DC and gate pulsed IV. The ratio of  $R_{on,pulse}/R_{on,DC}$  is 1.13, 1.03, 1.02, and 1.09 for the device without PMA, with 300, 400, and 500 °C PMA, respectively. The little increase of the  $R_{on,pulse}$  compared to the  $R_{on,DC}$  indicates good surface passivation effect of the  $\text{Al}_2\text{O}_3$ , and the negligible difference between the ratio of  $R_{on,pulse}/R_{on,DC}$  without PMA and that with various PMA conditions suggests good thermal stability of the effective  $\text{Al}_2\text{O}_3$  passivation.

Figure 4 shows the buffer leakage between two individual Ohmic pads with both width and gap of 100  $\mu\text{m}$  for samples without and with various PMA temperatures. The buffer leakage of a HEMT sample fabricated using the same epi wafer was added for comparison with the same PMA conditions. It can be seen that the buffer leakage currents for the MOSHEMT samples without PMA and with 300 and 400 °C PMA are three orders of magnitude higher than that of the HEMT sample with/without PMA. The significantly increased buffer

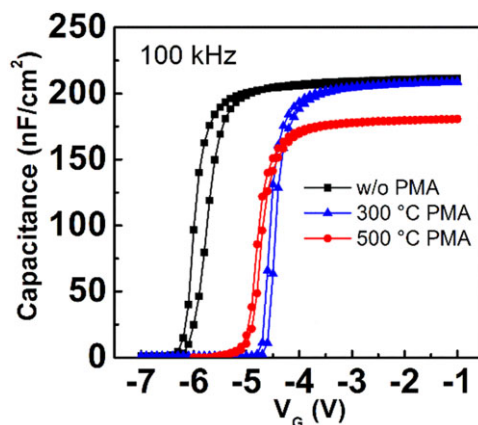


**Figure 4** Buffer leakage comparison of MOSHEMT and HEMT samples without and with various PMAs. The pad width and gap both are 100  $\mu\text{m}$ .

leakage mainly results from the surface leakage at the  $\text{Al}_2\text{O}_3$ /GaN interface. With PMA at 500 °C, the surface leakage can be reduced by more than one order of magnitude.

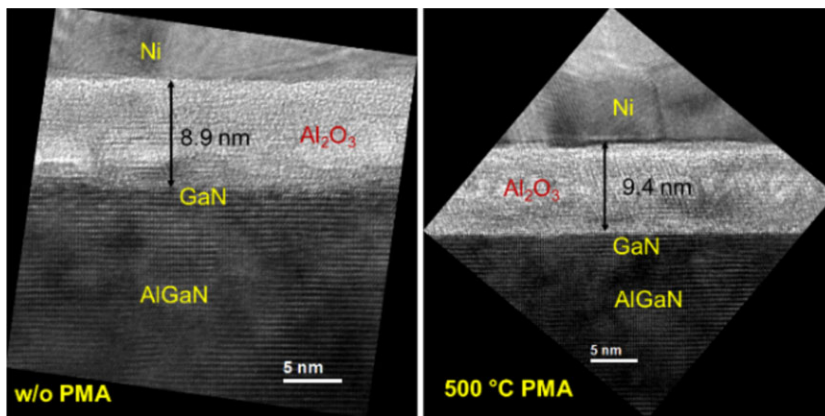
Double-sweep mode CV characteristics of the MOSCAPs on samples without PMA, with 300 °C PMA and with 500 °C PMA were shown in Fig. 5. The accumulation capacitance for the MOSCAP with 500 °C PMA is  $\sim 10\%$  lower than those without PMA and with 300 °C PMA. The reduction of the accumulation capacitance indicates the increase of equivalent oxide thickness (EOT). Moreover, the hysteresis in the CV of MOSCAPs can be reduced from  $\sim 0.2$  V without PMA to  $\sim 0.1$  V with 300 and 500 °C PMA, suggesting an improved interface after PMA. The reduction of the accumulation capacitance is also part of the reasons for the decrease of maximum drain current of MOSHEMTs with 500 °C PMA. It was suspected that the GaN surface had been oxidized during the high temperature annealing.

To compare the oxide thicknesses for samples without and with 500 °C PMA, two samples were prepared with 10 nm  $\text{Al}_2\text{O}_3$  and 20 nm Ni on top for TEM observation. PMA at 500 °C was performed for one of them. The cross-sectional TEM images for the two samples are shown in



**Figure 5** Capacitance–voltage characteristics of circular MOSCAPs without and with various PMAs.





**Figure 6** Cross-sectional TEM images for samples without PMA and with 500 °C PMA.

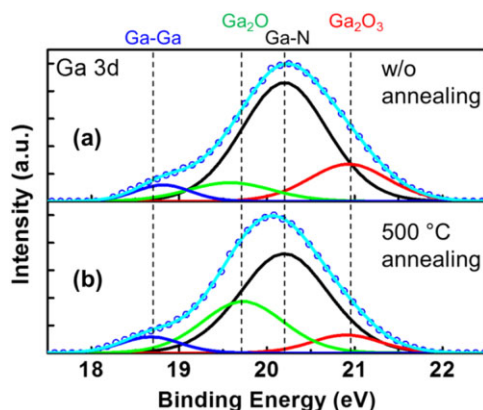
Fig. 6. The oxide layer thickness increases slightly from 8.9 to 9.4 nm and the interface of  $\text{Al}_2\text{O}_3/\text{GaN}$  is more abrupt after 500 °C PMA.

To further verify the oxidation process during the 500 °C PMA, the chemical bonding composition at the  $\text{Al}_2\text{O}_3/\text{GaN}$  interfaces was revealed by XPS, using a monochromatic Al  $K_\alpha$  radiation source ( $h\nu = 1486.6 \text{ eV}$ ). Two  $\text{GaN}/\text{AlGaN}/\text{GaN}$  samples with 2 nm  $\text{Al}_2\text{O}_3$  on top were prepared. After  $\text{Al}_2\text{O}_3$  deposition, one of the two samples was annealed at 500 °C in  $\text{N}_2$  ambient for 10 min by RTA (500 °C PMA condition). Figure 7 shows the Ga 3d core-level spectra of the two samples. The peaks are de-convoluted into four major components attributed to Ga–Ga,  $\text{Ga}^+-\text{O}$  ( $\text{Ga}_2\text{O}$ ), Ga–N, and  $\text{Ga}^{3+}-\text{O}$  ( $\text{Ga}_2\text{O}_3$ ) [17]. The two oxidation states  $\text{Ga}_2\text{O}$  and  $\text{Ga}_2\text{O}_3$  contribute together to the Ga–O bond component. By calculating the percentage of each component, the Ga–O/Ga–N bond ratio was found increased from 0.32 to 0.62 after 500 °C annealing. The increase of Ga–O/Ga–N bond ratio indicates the oxidation process at the  $\text{Al}_2\text{O}_3/\text{GaN}$  interface during the high temperature annealing. The significant increased Ga 1+

oxidation state suggests the formation of a thin  $\text{Ga}_2\text{O}$  interfacial layer, which was believed to give rise to a lower defect density and favorable impact on surface passivation [18]. Therefore, the 2D-VRH conduction, which was regarded as the mechanism of surface leakage in passivated GaN HEMTs [11], can be suppressed. Consequently, the  $I_{\text{off}}$  can be significantly reduced.

**4 Conclusions** The impact of PMA on the  $I_{\text{off}}$  for GaN MOSHEMTs on Si has been investigated in this study. It is found that the  $I_{\text{off}}$  can be reduced by three orders of magnitude with PMA at 500 °C in  $\text{N}_2$  for 10 min. The reduction of  $I_{\text{off}}$  results from the suppression of surface leakage, which is achieved by the surface oxidation process at the interface of  $\text{Al}_2\text{O}_3/\text{GaN}$  during the high temperature annealing.

**Acknowledgements** This work was supported by the Research Grants Council (RGC) theme-based research scheme (TRS) of the Hong Kong Special Administration Region Government under grant T23-612/12-R. Technical supports from Nanoelectronics Fabrication Facility (NFF) and Materials Characterization and Preparation Facility (MCPF) at HKUST were also acknowledged.



**Figure 7** Ga 3d core-level spectra at the  $\text{Al}_2\text{O}_3/\text{GaN}$  interface of the  $\text{Al}_2\text{O}_3/\text{GaN}/\text{AlGaN}/\text{GaN}$  samples (a) without annealing and (b) with 500 °C annealing. Each measured spectrum (blue circle symbol) was de-convoluted into four major components (solid lines) corresponding to Ga–Ga (blue),  $\text{Ga}_2\text{O}$  (green), Ga–N (black), and  $\text{Ga}_2\text{O}_3$  (red).

## References

- [1] Y. Wu, M. Jacob-Mitos, M. L. Moore, and S. Heikman, *IEEE Electron Device Lett.* **29**(8), 824 (2008).
- [2] J. W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, *IEEE Electron Device Lett.* **31**(3), 195 (2010).
- [3] D. Xu, K. K. Chu, J. A. Diaz, M. Ashman, J. J. Komiak, L. M. Pleasant, C. Creamer, K. Nichols, K. H. G. Duh, P. M. Smith, P. C. Chao, L. Dong, and P. D. Ye, *IEEE Electron Device Lett.* **36**(5), 442 (2015).
- [4] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, and V. Sahmuganathan, *Appl. Phys. Lett.* **95**(22), 223501 (2009).
- [5] T. Huang, X. Zhu, K. M. Wong, and K. M. Lau, *IEEE Electron Device Lett.* **33**(2), 212 (2012).
- [6] T. Hashizume, S. Ootomo, and H. Hasegawa, *Appl. Phys. Lett.* **83**(14), 2952 (2003).
- [7] J. J. Freedman, T. Kubo, and T. Egawa, *IEEE Trans. Electron Devices* **60**(10), 3079 (2013).

- [8] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, and D. Jena, *Appl. Phys. Lett.* **99**(19), 193504 (2011).
- [9] N. Ramanan, B. Lee, and V. Misra, *Appl. Phys. Lett.* **106**(24), 243503 (2015).
- [10] Z. H. Liu, G. I. Ng, H. Zhou, S. Arulkumaran, and Y. K. T. Maung, *Appl. Phys. Lett.* **98**(11), 113506 (2011).
- [11] Y. Chen, K. Zhang, M. Cao, S. Zhao, J. Zhang, X. Ma, and Y. Hao, *Appl. Phys. Lett.* **104**(15), 153509 (2014).
- [12] T.-H. Hung, S. Krishnamoorthy, M. Esposto, D. N. Nath, P. S. Park, and S. Rajan, *Appl. Phys. Lett.* **102**(7), 072105 (2013).
- [13] T.-H. Hung, P. S. Park, S. Krishnamoorthy, D. N. Nath, and S. Rajan, *IEEE Electron Device Lett.* **35**(3), 312 (2014).
- [14] Z. Xu, J. Wang, Y. Cai, J. Liu, C. Jin, Z. Yang, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, J. Zhang, and Y. Hao, *IEEE Electron Device Lett.* **35**(12), 1200 (2014).
- [15] T. Huang, X. Zhu, and K. M. Lau, *IEEE Electron Device Lett.* **33**(8), 1123 (2012).
- [16] T. Huang, K. M. Wong, M. Li, X. Zhu, and K. M. Lau, *Phys. Status Solidi C* **9**(3–4), 919 (2012).
- [17] M. Mishra, S. Krishna, T. C. N. Aggarwal, M. Kaur, S. Singh, and G. Gupta, *Phys. Chem. Chem. Phys.* **17**(23), 15201 (2015).
- [18] C. L. Hinkle, M. Milojevic, B. Brennan, A. M. Sonnet, F. S. Aguirre-Tostado, G. J. Hughes, E. M. Vogel, and R. M. Wallace, *Appl. Phys. Lett.* **94**(16), 162101 (2009).